“Signal Integrity Analysis in the Open Architecture”

By

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Wavecrest is proud to be a charter member of the Semiconductor Test Consortium. For the last 8 years Wavecrest has played a leadership role in signal integrity analysis with various standards [4] groups. This expertise has led us to develop IP useful in the analysis of fast data signals.

Integration plan:
Wavecrest has a two-phase plan to integrate the SIA-3000 into the OPENSTAR™ platform. The first phase is to integrate the engineering & characterization software tools called Gigaview™ onto the PC system controller along with the Production API library. With the SIA-3000 software tools in the OPENSTAR™ the SIA-3000 hardware can now be used with the OPENSTAR™ system for Signal Integrity & Jitter Analysis of customers devices.

The second phase will include shrinking the SIA-3000 hardware onto a test head module. This will enable OPENSTAR™ customers to have 6GHz bandwidth signal integrity analysis and jitter analysis close to the device under test.

End Application:
- The SIA-3000 will be used to characterize the next generation of PCI-Express bus running at 5.0Gbps.
- Will be used to verify compliance to the standards for all forms of SERDES interfaces such as XAUI, GBE, 2x, 3x, 4x Fibre’ Channel, 2.5Gbps InfiniBand, PCI-Express, Serial ATA, OC-48 and many others.
- Will be used for FAST production as well as detailed characterization of SERDES and source synchronous interfaces.
- Will do clock and PLL devices analysis for engineering and high volume production.
- Will do “Eye Diagram” signal analysis with the 6GHz bandwidth ETO sampling scope.

What is the issue?
Today’s SoC ATE system must have the capability of testing SERDES and all forms of asynchronous interfaces to the latest ANSI and IEEE specifications. These new standards require BER or equivalent BER testing to 10⁻¹². That means to use today’s ATE system pin card comparator to test a XAUI DUT would require over 300 seconds test time to verify to the Total Jitter timing specification [1] at a BER of 10⁻¹². The SIA-3000 can perform these tests on the DUT and help debug the DUT test program.
- Design characterization and debug.
- Test program development and debug.
- Fast production testing to a BER of 10⁻¹² in <150ms
- Analyze signal waveforms, Tr/TF, Pw, Per, etc…

How does OPENSTAR™ help the customer?
Wavecrest has patented several ways to deconvolve the timing distribution of a signal edge into its basic parts. This equivalent BER method is very fast making SoC testing to compliant specifications possible.
- Autocorrelation enables the following [3]
  - Measures out of phase jitter noise.
  - Power spectral density
  - Gaussian jitter
  - Periodic jitter
- Tailfit™ enables the following [2]
  - Separate deterministic timing from pdf.
  - Separate Gaussian components from pdf.
- Auto Arming to pattern enables the following [3]
  - Directly measure DDJ or ISI of signal.
  - Measure DDJ transition density.
  - Simulate 1st order PLL CDR.

The Wavecrest products for OPENSTAR™:
- SIA-3000TM hardware.
  - 6GHz ETO sampling scope
  - PLL CDR for eye diagrams
  - 10 differential channels
  - 6.25 Gbps TIA timing jitter analysis.
- GigaView™ engineering & design tools
  - Enable DUT characterization on ATE
  - Plot and graphics tools
  - Plot interpreter tools for instant help.
  - Correlation to bench data.
- Production API libraries:
  - Simplifies complex test program gen.
  - Optimizes test program for speed.
  - Enables fast production testing.

Summary:
In phase two of the integration of the SIA-3000 into the OPENSTAR™ test system the user will be able to increase the number of differential pins by adding test modules to the test head. In the future, timing and signal analysis at even higher speeds is planned as well as lower cost capability at slower speeds as devices move into high volume production.

References: