Keynotes

Monday - Performance is Overrated or: How I Stopped Worrying and Learned to Love Slow Hardware
Speaker: Tim Sherwood (University of California, Santa Barbera)

Abstract – Processor performance has doubled many many times over during the past 40 years, but the very techniques used to achieve these performance gains have made it increasingly difficult to build software systems with critical properties such as security, determinism, real-time, non-interference, debuggability, and correctness. As we continue our march towards increasingly complex and heterogeneous chips, with more and more hidden state (e.g., predictors, caches, modes, accelerators), these properties are only becoming harder to realize. This fact significantly impedes progress in the development of our most safety-critical embedded systems such as those found in medical, avionic, and automotive systems. What if we started from scratch? What if we reconsidered system architecture from the gates up with an eye, first and foremost, towards the properties necessary to build reliable and trustworthy computing systems? Even if, in the end, we don't want to abandon performance and/or legacy infrastructure, can the lessons learned from this “gates up” thinking then be applied in practice to existing systems? Professor Sherwood will describe his experience with this approach around two important properties (security and correctness) and his experience transitioning ideas from basic research through to practical commercial products.

Speaker Bio – Tim Sherwood is a Professor of Computer Science and the Associate Vice Chancellor for Research at UC Santa Barbara. He is a 7-time winner of the IEEE Micro Top Pick Award, the co-founder of the hardware security startup Tortuga Logic, an ACM Distinguished Scientist, winner of the UCSB Academic Senate Distinguished Teaching Award, and is the 2016 SIGARCH Maurice Wilkes Awardee "for contributions to novel program analysis advancing architectural modeling and security".

Tuesday - Amazon F1 Cloud-Based FPGAs
Speaker: David Pellerin (Amazon Web Services)

Abstract – The availability of FPGA-accelerated cloud services, combined with improved FPGA programming tools, is enabling a new generation of reconfigurable computing researchers and commercial application developers. This keynote session provides a technical overview of the F1 FPGA cloud-based instances, and walks through a typical development and deployment process including details of the FPGA hardware interfaces and software APIs. The session also includes information about the AWS Marketplace that allows FPGA applications to be secured, distributed, and monetized.

Speaker Bio – David Pellerin is Business Development Principal for High Performance Computing at AWS, with a focus on high-scale applications in engineering, manufacturing, financial services, life sciences, media, and energy. Prior to joining AWS, Mr. Pellerin had a career in electronic design automation and FPGA-accelerated computing. He has experience with circuit simulation and synthesis, grid and cluster computing, and embedded systems. Mr. Pellerin is the author of five Prentice Hall technical books including Practical Design Using Programmable Logic and Practical FPGA Programming in C.