ASAP 2015 Program

Monday - July 27, 2015

8:50 - 9:00 Opening Remarks

9:00 - 10:00 Keynote 1
Arvind, "BlueDBM: A Multi-access, Distributed Flash Store for Big Data Analytics"

10:00 - 10:30 Break

10:30 - 12:15 Session M1: Architecture and Technologies 1

Regular Papers:

Cecilia Gonzalez-Alvarez, Jennifer Sartor, Carlos Alvarez, Daniel Jimenez-Gonzalez and Lieven Eeckhout, "Automatic Design of Domain-Specific Instructions for Low-Power Processors"

Nachiket Kapre, "Custom FPGA-based Soft-Processors for Sparse Graph Acceleration"

Raphael Polig, Heiner Giefer and Walter Stechele, "A Soft-Core Processor Array for Relational Operators"

Short Papers:

Nasim Farahini and Ahmed Hemani, "Atomic Stream Computation Unit based on Micro-thread Level Parallelism"

Tanvir Ahmed and Yuko Hara-Azumi, "Timing Speculation-Aware Instruction Set Extension for Resource-Constrained Embedded Systems"

12:15 - 13:30 Lunch Break

13:30 - 15:00 Session M2: Application Acceleration 1

Regular Papers:

Nolan Denman, Mandana Amiei, Kevin Bandura, Liam Connor, Matt Dobbs, Mateus Fandino, Mark Halpern, Adam D. Hinch, Gary Hinshaw, Carolin Hofer, Peter Klages, Kyonshi Masui, Juan Mena Parra, Laura Newburgh, Andre Recnik, Richard Shaw, Kris Sigurdson, Kendrick Smith and Keith Vanderlinde, "A GPU-based Correlator X-engine Implemented on the CHIME Pathfinder"


Tahsin Reza, Aaron Zimmer, Parwant Ghuman, Tanuj Kr Aasawat and Matei Ripeanu, "Accelerating Persistent Scatterer Pixel Selection for InSAR Processing"

Short Paper:

Peter Klages, Ue-Li Pen and Keith Vanderlinde, "An Efficient Real-time Data Pipeline for the CHIME Pathfinder"

15:00 - 16:00 Break and Poster Session 1

Ross Thompson and James Stine, "An IEEE 754 Double-Precision Floating-Point Multiplier for Denormalized and Normalized Floating-Point Numbers"

Wei He and Dirmanto Jap, "Dual-Rail Active Protection System against Side-Channel Analysis in FPGAs"

Tung Hoang Thanh, Amrati Shamshayati, Henry Hoffmann and Andrew A. Chien, "Does Arithmetic Logic Dominate Data Movement? A Systematic Comparison of Energy-Efficiency for FFT Accelerators"

Bingzhe Li, M. Hassan Najafi and David Lilja, "An FPGA Implementation of a Restricted Boltzmann Machine Classifier Using Stochastic Bit Streams"

Mehmet Ali Arslan, Ravian Gruian and Krzysztof Kuchcinski, "Application-Set Driven Exploration for Custom Processor Architectures"

Abdelhamid Bine, Abdelazif Elouardj, Bastien Vincde and Samir Bouaziz, "Speeding up Graph-based SLAM Algorithm: a GPU-based Heterogeneous Architecture Study"

16:00 - 17:15 Session M3: Arithmetic

Regular Papers:

Hugues de Lassus Saint-Geniès, David Defour and Guillaume Revy, "Range Reduction Based on Pythagorean Triples for Trigonometric Function Evaluation"

Yongchao Liu and Bertil Schmidt, "LightSpMV: Faster CSR-based Sparse Matrix-Vector Multiplication on CUDA-enabled GPUs"

Ran Zheng, Wei Wang, Hai Jin, Song Wu, Yong Chen and Han Jiang, "GPU-based Multifrontal Optimizing Method in Sparse Cholesky Factorization"

17:30 - 19:30 Opening Day Reception on Patio of University of Toronto Faculty Club
continues...
Tuesday - July 28, 2015

9:00 - 10:00  **Keynote**
Derek Chiou, *Accelerating Data Centers with Reconfigurable Logic*

10:00 - 10:30  **Break**

10:30 - 11:40  **Session T1: Architecture and Technologies 2**

**Regular Paper:**
Seiichi Tade, Hiroki Matsutani, Hideharu Amano and Michihito Koibuchi, "A Metamorphic Network-on-Chip for Various Types of Parallel Applications"

**Short Papers:**
Ming-Ju Wu, Yan-Ting Chen and Chan-Jen Tsa, "Dynamic Pipeline-Partitioned Video Decoding on Symmetric Stream Multiprocessors"
Ran Wang, Jie Han, Bruce Cockburn and Duncan Elliott, "Stochastic Circuit Design and Performance Evaluation of Vector Quantization"

11:40 - 11:50  **Introduction Presentation to ASAP 2016**

11:50 - 13:00  **Lunch Break**

13:00 - 14:45  **Session T2: Crypto/Security**

**Regular Papers:**
Mihai Maruseac, Gabriel Ghinita, Ming Ouyang and Razvan Rughinis, "Hardware Acceleration of Private Information Retrieval Protocols Using GPUs"
Moon Sung Lee, Yongge Lee, Jung Hee Cheon and Yunheung Paek, "Accelerating Bootstrapping in FHEW using GPUs"

**Short Papers:**
Pei Luo, Liwei Zhang, Yunsi Fei and A. Adam Ding, "Towards Secure Cryptographic Software Implementation Against Side-Channel Power Analysis Attacks"
Paolo Martim, Lexie Sousa, Julien Eynard and Jean-Claude Bajard, "Programmable RNS Lattice-Based Parallel Cryptographic Decryption"

14:45 - 15:45  **Break and Poster Session 2**

Xin Fang, Pei Luo, Yunsi Fei and Miriam Leeser, "Balance Power Leakage to Fight Against Side-Channel Analysis at Gate Level in FPGAs"
Jie Tang, Chen Liu and Jean-Luc Gaudiot, "How can Garbage Collection be Energy Efficient by Dynamic Offloading?"
Zhinan Cheng, Xi Li, Ilie-iun Sun, Gr-Gao and Jiachen Song, "Automatic Frame Rate-Based DVFS Of Game"
Rodrigo Devigo, Liana Duenha, Rodolfo Azevedo and Ricardo Santos, "MultiExplorer: A Tool Set for MultiCore System-on-Chip Design Exploration"
Vincenzo Catania, Andrea Mines, Salvatore Monteleone, Maurizio Palesi and Davide Patti, "Noxim: An Open, Extensible and Cycle-accurate Network on Chip Simulator"
Peter Klages, Kevin Bandura, Nolan Denman, Andre Recnık, Jonathan Sievers and Keith Vanderlinde, "GPU Kernels for High-Speed 4-bit Astrophysical Data Processing"

15:45 - 17:15  **Session T3: Tools and Design Methodologies**

**Regular Papers:**
Moritz Schmid, Oliver Reiche, Frank Hannig and Jürgen Teich, "Loop Coarsening in C-based High-Level Synthesis"
Dylan Rudolph and Greg Stitt, "An Interpolation-Based Approach to Multi-Parameter Performance Modeling for Heterogeneous Systems"
Erkan Diken, Martin O’riordan, Róel Jordans, Lech Juswiak, Henk Corporaal and David Mokney, "Mixed-Length SIMD Code Generation for VLIW Architectures with Multiple Native Vector-Widths"

**Short Paper:**
Kenneth Hill, Stefan Craciun, Alan George and Herman Lam, "Comparative Analysis of OpenCL vs. HDL with Image-Processing Kernels on Stratix-V FPGA"

19:00 - 19:30  **Boarding for Boat**

19:30 - 20:00  **Boat Departs**

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Wednesday - July 29, 2015

9:00  9:50  Session W1: Fault Tolerance

Regular Papers:

Alexandru Tanase, Michael Witterauff, Jürgen Teich, Frank Hannig and Vahid Lari, "On-Demand Fault-Tolerant Loop Processing on Massively Parallel Processor Arrays"

Aniruddha Shastri, Greg Stitt and Eduardo Riccio, "A Scheduling and Binding Heuristic for High-Level Synthesis of Fault-Tolerant FPGA Applications"

9:50 - 10:20  Break

10:20  12:05  Session W2: Application Acceleration 2 and Power

Regular Papers:

Andreea Ingrid Funie, Paul Grigoras, Pavel Burnovskiy, Wayne Luk and Mark Salmon, "Reconfigurable Acceleration of Fitness Evaluation in Trading Strategies"

Hamed Tabkh, Majid Sabbagh and Gunar Schirner, "An Efficient Architecture Solution for Low-Power Real-Time Background Subtraction"

Shijie Zhou, Yun Qu and Viktor Prasanna, "Large-scale packet classification on FPGA"

Short Papers:

Andrew Wong, Saied Hemati and Warren Gross, "Efficient Implementation of Structured Long Block-Length LDPC Codes"

Andrea Sanny, Yi-Hua Edward Yang and Viktor Prasanna, "Energy Optimization of Parallel k-Means Clustering Algorithm on FPGA"

12:05 - 12:15  Closing Remarks