Abstract
Due to power and performance reasons, MPSoC architectures are getting widespread in virtually all domains of computing. Their HW/SW design constraints are particularly tight in wireless communication devices. The amount of mobile data traffic is expected to grow by 1000x within the next decade, resulting in very high performance requirements. At the same time, especially in battery driven devices, maximum energy efficiency is a must. Moreover, the problem of how to efficiently implement software on embedded parallel processor architectures is largely unsolved today. This keynote covers several novel system-level design technologies, conceived to help in efficient HW/SW design for multi-billion transistor embedded multicore platforms, with emphasis on the special demands of wireless applications. We will provide an introduction to automated design of application specific processors as the key MPSoC building blocks. Next, we will discuss some recent advances in virtual prototyping and high-speed simulation of complex architectures and entire devices. Furthermore, we will sketch the MAPS compiler approach for mapping embedded application software onto heterogeneous parallel target platforms. Finally, we provide an outlook on further key research issues in embedded systems design to support the future "mobile society".

Biography
Rainer Leupers received the M.Sc. (Dipl.-Inform.) and Ph.D. (Dr. rer. nat.) degrees in Computer Science with honors from the Technical University of Dortmund, Germany, in 1992 and 1997. From 1997-2001 he was the chief engineer at the Embedded Systems chair at TU Dortmund. During 1999-2001 he was also a team leader at ICD, where he headed industrial specific service projects. In 2002, Dr. Leupers joined RWTH Aachen University as a professor for Software for Systems on Silicon. Since then, he has also been a visiting faculty member at the ALARI Institute in Lugano. His research and teaching activities comprise software development tools, processor architectures, and electronic design automation for embedded systems, with emphasis on multiprocessor systems-on-chip. He published numerous books and technical papers, and he served as program committee member and topic chair of leading international conferences, including DAC, DATE, and ICCAD. He was a co-chair of the MPSoC Forum and SCOPES. Dr. Leupers received several scientific awards, including Best Paper Awards at DATE 2000, 2008 and DAC 2002, and he holds several patents on processor design automation technologies. He has been a co-founder of LISATek, an EDA tool provider for embedded processor design, now part of Synopsys Inc. He has served as consultant for various companies, as an expert for the European Commission, and in the management boards of compound research projects like UMIC, HiPEAC, and ARTIST.
Reconfigurable Computing for Statistical Physics:
The Weird Case of JANUS

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Abstract
The numerical simulation of complex physical systems has evolved into a key investigation tool for physicists as well as a grand challenge of high performance computing. Several areas of computational physics -- Quantum Chromodynamics, Computational Fluid Dynamics, the evolution of Gravitational Systems, the simulation of highly non-linear systems -- have been at the forefront of this trend in the last two or three decades; over the years, several application-driven special architectures have been developed to provide -- efficiently and cheaply -- computing power to these applications. From the point of view of computer architecture, these systems are characterized by a very close match between algorithm and machine structure, that in turn allows a very effective exploitation of the large degree of parallelism usually found in the corresponding numerical algorithms. Some of the ideas developed in these machines have been later adopted in commercial systems. This talk will describe recent activity along these lines brought forward by the JANUS and JANUS2 projects. These projects have developed a simulation environment to study spin systems -- relevant in condensed matter physics -- based on a reconfigurable architecture based on FPGAs. For the physicists, these systems provide computing power larger by a factor 100x than available on state-of-the-art commercial solutions; for the computer scientist, they are an interesting example of the potentially huge rewards of an application-driven massively many-core structure coupled to a low-latency memory system. The talk will i) briefly introduce the physics computational problem, ii) describe the JANUS and JANUS2 systems, iii) present performance results and iv) compare with other possible approaches.

Biography
Raffaele Tripiccione (born 1956) obtained his laurea degree in Physics from the University of Pisa. He carried out his doctoral studies at Scuola Normale Superiore in Pisa. He spent his early scientific career at Istituto Nazionale di Fisica Nucleare (INFN). He moved to the Università di Ferrara, as a full professor of physics, in the year 2000. Over the years he has visited for extended periods several scientific institutions, such as Fermilab in the US and CERN (Geneva, Switzerland). He has supervised approximately 20 doctoral theses and a large number of master theses. His research interests are in the area of computational theoretical physics. Over the years he has focused his work on Lattice Gauge Theories (LGT), turbulent fluid dynamics and complex systems (mainly spin-glasses). He has played a major role in the development of several application-driven high performance computer systems for physics applications. He is one of the founders of the French-German-Italian APE project, that has developed several generation of LGToptimized computer system. He has been the head of the project from 1990 to 2000; he also collaborated to the development of the QPACE machine, that has been recently the top entry of the Green500 list. Currently, he is involved in the JANUS/JANSU2 projects, that have developed reconfigurable computer systems strongly optimized for the simulation of complex systems, mainly in condensed-matter physics.
Designing Ultra Low Power SIMD Processors

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Abstract
Emerging embedded systems, like smart phones and cyber-physical systems, often require high computational performance. On the other hand, such systems typically have a limited power source like batteries or solar panels. Therefore, energy-awareness becomes an increasingly important concept in processor design for embedded systems.

To deal with energy-efficiency in combination with high performance requirements, we will outline in this presentation a Single-Instruction-Multiple Data (SIMD) processor. In many embedded applications, substantial amounts of data-level parallelism can be exploited. The inherent low power nature of a massively parallel SIMD architecture makes it very suitable for building efficient embedded processing systems. Aggressive VDD scaling can be exploited to improve the energy balance in case (temporarily) less performance is required.

To raise the efficiency even further, optimizations at various levels of the processor architecture are required. We propose 4 optimizations which are applied to the SIMD processing elements: 1) exploiting locality; 2) the explicit datapath in Transport Triggered Architecture (TTA) is used, which exposes much more details to the software than conventional processors, allowing the compiler to generate energy efficient codes; 3) a reconfigurable special function unit is employed, which allows different applications to use different custom instruction that can greatly improve energy efficiency; 4) an energy aware methodology is used in function unit design; in particular, the multiplier is able to operate in different modes depending on the effective width of the input data.

The proposed SIMD processor aims at 1pJ/op for typical embedded streaming applications. It will be the core component in a wide range of low power embedded computation systems.

Biography
Henk Corporaal has gained an MSc in Theoretical Physics from the University of Groningen, and a PhD in Electrical Engineering, in the area of Computer Architecture, from Delft University of Technology. Corporaal has been assistant and associate professor at the Delft University of Technology in the field of computer architecture and code generation, had a joint professor appointment at the National University of Singapore, and has been scientific director of the joined NUS-TUE Design Technology Institute. He also has been department head and chief scientist within the DESICS (Design Technology for Integrated Information and Communication Systems) division at IMEC, Leuven (Belgium). Furthermore, Corporaal has been teaching at several schools for higher education. Currently Corporaal is Professor in Embedded System Architectures at the Eindhoven University of Technology (TU/e) in The Netherlands. He has co-authored over 300 journal and conference papers in the (multi-)processor architecture and embedded system design area. Furthermore he invented a new class of VLIW architectures, the Transport Triggered Architectures, which is used in several commercial products, and by many research groups. His current research projects are on single and multi-processor architectures and the predictable design of soft- and hard real-time systems. This includes research and design of embedded system architectures, being low power and exploiting all kinds of parallelism, and the (semi-)automated mapping of applications to these architectures. For further details see his website at corporaal