MULTIBUS® continues to evolve to meet the challenges of the VLSI revolution

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ABSTRACT

MULTIBUS is the world’s most popular microprocessor system architecture. The success of the MULTIBUS is attributable to its compatible evolution, always meeting the demands of new VLSI microprocessors without forsaking compatibility with existing products. New system architecture’s need for the use of large amounts of high performance memory is the motivation for continued MULTIBUS evolution. This need is addressed through the introduction of the Local Bus Extension (iLBX™). Whereas the local bus under the previous definition was physically limited to on-board execution, the iLBX evolution allows the local bus to span up to five separate boards. The benefit of the LBX is the ability to achieve on-board performance when operating out of physically separate boards. Intel’s iSBC® 286/10 single board computer combines the latest VLSI with the iLBX extension, creating a new level of microcomputer system performance. This new board vividly demonstrates that the MULTIBUS continues to evolve to meet the challenges of the VLSI revolution.
BACKGROUND

The MULTIBUS system architecture was developed in 1975 by Intel Corporation to make microprocessors easier to use. The original MULTIBUS contained three unique qualities that have differentiated the MULTIBUS systems from traditional computer systems.

The first of these qualities is its standardization. The MULTIBUS specification (IEEE 796) is precise enough so that MULTIBUS boards from different vendors are fully compatible. The second MULTIBUS quality is multiprocessing—the ability to have multiple CPU boards in one system. This ability is the basis for distributed processing and allows a complex design to be built from easily managed modules. The third quality is the MULTIBUS' generality. The architecture is designed to accommodate any and all microprocessors, and all popular CPUs have been adopted to the MULTIBUS. Intel has encouraged other vendors to use the MULTIBUS by providing specifications, applications notes, and even bus interface ICs.

The popularity of the MULTIBUS has been phenomenal. Over two million MULTIBUS compatible boards are in use today. There are now approximately 120 vendors providing 1,300 different MULTIBUS compatible products. The advantages of such a widespread standard acceptance can be summarized as better products for less cost.

AN EVOLVING STANDARD

The MULTIBUS standard has evolved many times to accommodate the rapidly advancing microprocessors. The long-term success of the MULTIBUS is attributable to its compatible evolution, always meeting the demands of new VLSI microprocessors without forsaking compatibility with existing products. MULTIBUS evolution has been both structural and architectural. Structural evolution has allowed the bus to support new CPU capabilities (Adding address lines to accommodate 24-bit addressing). Architectural evolution (see Figure 1) enhances the MULTIBUS design philosophy of functional partitioning within loosely coupled distributed processing systems.

The VLSI revolution is continuing with even more powerful microprocessors on the horizon. These microprocessors present new challenges to the MULTIBUS. The most pressing challenge is the architectural need for large amounts of high performance memory. As in the past, the MULTIBUS has evolved to meet this need while maintaining compatibility with the existing MULTIBUS family.

LOCAL BUS EXTENSION

Microcomputer system memory size requirements have grown faster than VLSI technology. Applications were rarely larger than 32 kilobytes four years ago; applications of the future will utilize several megabytes of memory. This 100 times increase in memory demand has occurred over the same period as a 16 times increase in memory chip density. The result is that more board space is required for microprocessor system memory than ever before (see Figure 2).

As the need for more memory was mounting, the performance disparity between on-board (or local) memory and...
off-board memory was growing (see Figure 3). In 1975, processor boards ran equally fast from off-board memory as from local memory. Today's high performance processor boards, however, run (worst case) two times faster in local memory than in off-board memory. This performance disparity has lead MULTIBUS board vendors to design boards with increasing amounts of local memory. The demand for even larger amounts of local memory combined with the physical board space limitations is the motivation for architectural evolution of the MULTIBUS.

The local bus extension to the MULTIBUS architecture extends the concept of the local bus. Whereas the local bus under the previous definition was physically limited to on-board, the iLBX evolution allows the local bus to span up to five separate boards. The benefit of the iLBX extension is the ability to achieve local performance when operating out of physically separate boards.

The iLBX extension not only provides tremendous performance benefits, but also maintains compatibility with previous MULTIBUS products. The iLBX physical connections are on the P2 connector of the MULTIBUS card. The lines of the P2 connector used for the iLBX were previously declared Reserved, not bussed. But even custom board designers who have used these lines need not worry. The iLBX concept groups a CPU board with several memory boards into a virtual SBC (see Figure 4). Therefore only the logical group that supports the iLBX is connected together. The full iLBX specification is publicly available today, and the first boards that support the iLBX extensions are now being shipped by Intel Corporation (see Figure 5).

THE LATEST PRODUCT

The iSBC® 286/10 Single Board Computer combines the most advanced VLSI microprocessor with the enhanced MULTIBUS architecture. The performance of the combination is awesome. The iAPX 286 CPU is Intel's latest 16-bit microprocessor implemented with 130,000 transistors on one chip. This CPU performs many internal functions, including memory management and protection, in parallel thus executing instructions in less clock states. By using less states for execution, the iAPX 286 CPU accentuates the effect of memory overhead, known as wait states.

The iLBX bus provides the architectural solution by allowing iLBX memory performance to equal on-board performance. A fastest instruction analysis of the high performance iSBC 86/30 board versus the iSBC 286/10 board vividly illustrates the combined effects of the iAPX 286 and iLBX combination (see Figure 6).

The fastest instruction analysis shows the performance advantage of the iAPX 286 CPU as 2 to 1 and the off-board memory overhead reduction (due to the iLBX architecture) as 3.5 to 1. The combined effect of these two positions the iSBC 286/10 in a new performance class for microcomputers.
CONCLUSIONS

New products like the iSBC 286/10 board prove that a standard architecture can successfully evolve to meet new challenges. The MULTIBUS standard is the world’s most popular microprocessor architecture greatly due to its compatible evolution. Future needs such as the accommodation of 32-bit microprocessors will necessitate the next evolution of MULTIBUS. Making changes to an industry standard is a difficult, but in this case, essential task. Each change runs the risk of destroying the MULTIBUS standard, but if managed correctly actually strengthens it. The MULTIBUS has endured many challenges since its inception and must continue to meet the new needs of the VLSI revolution.

<table>
<thead>
<tr>
<th>CPU INSTRUCTION</th>
<th>iSBC' 286/10 BOARD</th>
<th>iSBC' 86/30 BOARD</th>
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<tbody>
<tr>
<td>MEMORY OVERHEAD</td>
<td>2 (ON BOARD) - 7 (OFF BOARD)</td>
<td>2 (ON BOARD) - 2 (OFF BOARD)</td>
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<tr>
<td>TOTAL</td>
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