Semiconductor rams of the future

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Semiconductor memories have, since 1970, been a significant factor in data storage. This has been especially true in Random Access memories and is becoming true of the slower serial access memories.

The manufacture of semiconductor memories takes place in two stages; the batch manufacture of the dice as wafers and the piece-by-piece assembly of the good dice into packages. It is the batch manufacturing of the dice that has led to the continuing trend of lower cost per bit. (Figure 1) With each new generation of memories, four factors have contributed to increased density of good bits per batch and therefore lower cost. These four factors are; decrease in storage cell complexity, decrease in feature size, increase in wafer size (thus batch size), and decrease in defect density.

Decrease in storage cell complexity has been the most significant factor in increasing batch density. (Figure 2) An appropriate comparison of cell complexity can be made by expressing cell area in units of \( f^2 \), where \( f \) is the minimum feature size allowed by the pattern-definition technology.

Cell sizes in the last eight years have decreased from \( 200f^2 \) for the first static flip-flops to a present range of \( 16f^2 \) to \( 20f^2 \). It is theoretically possible to reach a cell size of \( 4f^2 \) where there are two features in both the X and Y directions, one to store the information and the other to isolate it from adjacent cells. If means can be found to isolate adjacent cells in less than a feature size, then a cell size of \( f^2 \) is possible.

Added to the decrease in cell size is an inherent increase in layout efficiency. When memory size increases by a factor of four, only twice as many decoders, sense amplifiers, etc., are required; only two more address buffer circuits and the same number or less bonding pads are needed.

A combination of design and process innovation has allowed this decrease in storage cell complexity, resulting in a 13.5 times increase in batch density.

The second most significant of the four factors has been increased wafer size. As a result of a significant amount of development work on the equipment for manufacturing raw wafers and processing wafers, as well as developing processing techniques for handling larger wafers, the size of wafers has increased from two inches to four inches in diameter. This has resulted in a four times increase in wafer area and therefore a four times increase in batch density.

The remaining two factors, feature size and defect density have contributed the least to increasing the number of good bits per batch. Smaller minimum feature sizes have been possible as a result of improvements in mask making, mask aligning, and photoresist technology. Full utilization of improvements has been hampered by several factors. As feature sizes approach the film thicknesses and step heights present, dimensional control and feature integrity becomes increasingly difficult to maintain. In addition, as the feature size is reduced, the size of particle that will cause a defect in the masking is also reduced. Since smaller particles have a much higher probability of passing through the various forms of filtering used in semiconductor manufacturing facilities, the effective density of defects increases exponentially with decreasing feature size. (Figure 3) These factors have limited batch density improvements due to feature size reduction to a 2.2 times increase.

Overall, these four factors have resulted in a 120 times increase in batch density. With each new generation of memories, when a four times larger memory could be fabricated and packaged for the same cost as four smaller memory in four packages, the new generation was introduced. The packaging density increase of course offered an overall savings in system costs and users started switching to the new generation. As volume has increased and yields improved, costs have dropped and the cycle has repeated.

To what extent can we extrapolate and thereby predict the future?

With respect to decreasing cell complexity, there is little real room for progress. Present design and process technology is producing cells in the \( 16f^2 \) to \( 20f^2 \) size range. If we attain a \( 4f^2 \) cell size, we will only realize a factor of four to five times density increase. In addition, in order to attain a \( 4f^2 \) cell size, significantly new device types will have to be developed or adjacent storage cells will have to be built on separate layers. Increasing the number of layers affects yield in the same manner as a larger area. Therefore, achieving a \( 4f^2 \) cell, with a corresponding increase in number of mask layers, may give no actual improvement in good bits per batch. Examples of new device types are Ovonic materials sandwiched between layers at the memory crosspoints or CCD devices which require changes in system architecture to cope with large percentages of their data base in serial access storage. In such cases the technology development required is significant.
most manufacturing lines. They have allowed the masks to become permanent tooling rather than production materials that must be discarded with every second or third run, and therefore, made it practical to invest in defect free masks with very tight tolerances. Projection aligners will allow feature sizes approaching one to two microns, a five times improvement over present practice. The lower defect densities possible with projection aligners will help offset the exponentially increasing effective defect density inherent with smaller feature size, but significant and costly improvements will also be needed to reduce other defect sources.

Electron Beam exposure systems are being developed, evaluated and purchased. Proponents of E.B. systems are claiming that they are about to revolutionize the industry. Proper analysis indicates that they will be a useful tool for mask making purposes, but their costs and throughput are such that feature size improvements they make possible will be offset by increased processing costs.

The industry is probably five to eight years away from the
time when the cost and throughput of E.B. systems will allow practical use in direct wafer manufacture.

Feature size reduction, alone, does not determine the size of features that will be used, only the lower limit available. The devices from which the circuits are constructed must be scaled within other physical constraints.

Theoretically, MOS transistors, for example, can be scaled to quarter micron feature size, but some device characteristics don’t scale well. As devices are scaled, circuit operating voltages and power densities must scale proportionately.

Such scaling requires re-engineering of device structures, process control, and film thicknesses. Parasitic parameters, such as leakage, noise, sub-threshold current, and sheet resistance do not scale as other circuit parameters and will require innovative design and/or materials research to deal with them.

Considering these factors then, it is theoretically possible for the batch density to increase by another 100 times in the next eight years. The task will require very large investments in capital and talent. The number of manufacturers able to make these investments will decrease. Moreover the market for memory products must continue to expand at a rate that will allow amortization of those investments.

It is appropriate at this point to apply this information to predictions of the coming generations of semiconductor memories.

In dynamic RAMs, MOS will dominate. The 16K will be the main production part through mid-1980. By mid-1980 significant quantities of 64K RAMs will be available. The 64K Dynamic RAMs will use scaled MOS devices (4 micron feature size), reduced power supply voltages (probably 5 Volts), 10\(\mu\) to 12\(\mu\) cell sizes, and be manufactured on 4 inch wafers. Some of these same techniques may be applied to the 16K RAMs but the cost of packaging four 16K RAMs will be offset by the lower cost of 64K RAMs, both for the manufacturer and for the user.

Storage cells for CCD memories are inherently easier to simplify and already 64K CCD’s with 5\(\mu\) cell sizes are close to reality. The disadvantages of serial memory storage will be offset by the lower cost per bit associated with CCD’s. Memory system and CPU manufacturers will accept the 5 to 10 percent throughput penalties in exchange for 1/5 to 1/3 the cost per bit CCD’s will offer.

MOS static RAMs will use scaled MOS to achieve data rates presently served by bipolar technology. They will be used predominantly to serve the IBM Add-on business until the problems of interfacing Dynamic RAMs to the new generations of machines are solved. Currently, 4K static RAMs are becoming readily available. By mid-1980 16K static RAMs will be readily available. Present CPU’s are implemented with ECL logic, and the translation from ECL to TTL levels to interface the RAMs adds appreciably to the access time. Future generations of MOS static RAMs will appear with ECL interfaces to eliminate the external level shifting and potentially reduce access times.

Bipolar static RAMs will continue to be the faster and smaller density memory devices. The bulk of the products will be ECL due to interfacing and access time requirements. Products will range from sub-five nanosecond 128-bit memories to sub-twenty-five nanosecond 4K bit memories. Cell sizes will be relatively large (120\(\mu\)^2) because of scaling difficulties and complex cell designs. Wafer size will be four inches. Device development will be concentrated towards reduction of parasitics (i.e., passive isolation) and increased gain band-width product of the transistors.
In summary, Bipolar static RAMs will move to higher speeds, MOS static RAMs will fill the speed range presently served by Bipolar RAMs (at lower cost and higher density), MOS Dynamic RAMs will be denser and lower in cost per bit, and CCD’s will extend the range of semiconductor memories in the direction of longer access time and lower cost per bit. (Figure 4) The investments in terms of talent and capital will be large for the manufacturers able to stay in the competition.

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