A multi-microprocessor ARES with associative processing capability on semantic data bases

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INTRODUCTION

Recent progress in architecture technology has had a great impact on the study of pattern recognition problems. The increase in processing power is bringing a new concept of "understanding" into recognition areas. Recognition objectives have been greatly extended to meet real social requirements. As observed in the speech recognition system developed at Carnegie-Mellon University, for example, efforts have been shifted from attaining higher recognition of isolated words to the implementation of a system which provides reasonable understanding of the more natural utterances of connected speech.

This system called HEARSAY provides multi-leveled knowledge sources ranging from parametric representations of the physical features of speech measured every 10ms to the conceptual level of common acceptance. Reliable performances for understanding speech are then attained by the hypothesize-and-test processes at these various levels where these knowledge sources are dynamically related to each other through a general structured global data base.

Concerning images, the University of Massachusetts is developing an image understanding system called VISIONS. The system transforms visual sensory numeric data to a symbolic structure representing a model of the image. Conceptual models which are not image-specific are stored as a knowledge source in the semantic data base and serve to specify the observed model by communicating with various levels of features hierarchically extracted through spatial windows of various sizes.

Both of the understanding systems (HEARSAY & VISIONS) are based on the principle of model construction (hypothesizing) and the deductive processing (testing) of conceptual models by the incorporation of a semantic data base (knowledge sources). Thus the associative search of all possible conceptual models on a semantic data base plays an important role in advanced pattern recognition systems, and the efficiency of the search becomes the dominant factor in attaining high performance.

An associative processor ARES proposed by the authors before also provides a powerful tool for associative search on semantic data bases in general because of the ability to associate data items on their deep structures. In the present paper, the association principle of ARES which is based on coding theory is generalized. The association capability is extended by the hierarchical use of a set of different codes. Following the overview of the generalized association mechanism is an architectural description of ARES which is now being developed. By adopting a multi-microprocessor organization, ARES has gained greater adaptability because of the functional flexibility provided by microprogramming.

In conclusion, the multi-microprocessor ARES provides an advanced pattern recognition facility partially bridging the gap between human cognitive behavior and logical processing by computers.

ADVANCED ASSOCIATION FACILITY

A semantic data base is defined generally as a collection of data items which are symbolic representations of speech or image. Data items D's are coded segmentally or categorically as shown in (1) in such a manner that the relatedness of the symbolic partial representations for each segmental or categorical block di is measured in terms of the distance of the code vectors associated with them.

\[
D = (d_{a1}, d_{a2}, \ldots, d_{ai}, \ldots, d_{an}), \quad 1 \leq i \leq p. \tag{1}
\]

The length of each segmental or categorical block di is not necessarily the same depending upon the application.

The association mechanism

Let's divide D into several blocks of equal length n as shown in (2), and apply an error correction scheme of the
Figure 1—Association process

From the collection of the Computer History Museum (www.computerhistory.org)
Hierarchical process of blurring

Let \((n, k, t)\) denote a code of length \(n\) which has \(k\) number of information digits with a \(t\)-error correction capability, and let the blurred data item derived from \(D\) by \((n_1, k_1, t_1)\)-code be represented as \(D_1 = e(D)\), where \(D_0 = D\). Suppose we want to have more general structure of data items, then we apply \((n_2, k_2, t_2)\)-code to \(D_1\) by dividing it into the blurring blocks of length \(n_2\). Thus we can proceed the blurring as indicated in (4) until we reach the blurredness required for the association, where the relation \(t_2 = 2t_1 - 1 + 1\) should necessarily be satisfied when \(n_2 \geq n_{s-1}\).

\[
D_0 \rightarrow D_1 = e_1(D_0) \rightarrow D_2 = e_2(D_1) \rightarrow \cdots \rightarrow D_s = e_s(D_{s-1}) \rightarrow \cdots
\]  

(4)

Association based on a deep structured relatedness

Content-addressing for the association can be applied at any level of blurring when the feature provided is satisfactorily general to meet the requirements. Let \(s^*\) denote the blurring level where content-addressing is applied. Then \(D_{s^*}\)’s in \(B_0\) to be associated are directly specified together with the related \(D_s\)’s (\(0 < s < s^*\)) when necessary, without tracing back the blurring processes to \(B_0\) since \(D_s\) (\(0 < s < s^*\)) and \(D_{s'}\) are stored in a one-to-one correspondence.

Figure 3 is a schematic diagram explaining how the content-addressing and hierarchical blurring are connected for performing association. The query item \(Q_0\) (\(eB_0\)) might in some cases be applied externally. The hit marks indicate the \(D_{s^*}\)’s which are content-addressed in \(B_{s^*}\). When we have a restriction on the number of associated data items, the
threshold $\theta$ for content-addressing is heuristically selected so that hit marks do not exceed a certain limit $\delta$.

ARES has data modification facility. Suppose $Q_0 (\in B_s)$ is given as a query item. If some $D_s$'s in $B_s$ are specified by $Q_0$ through the content-addressing at the blurring level $s^*$, these $D_s$'s and related $D_r$'s ($0 < s \leq s^*$) are replaced by $Q_0$ and its blurred expressions, respectively. Otherwise, $Q_r (0 \leq s \leq s^*)$ is registered, unmodified, to $B_s$ ($0 \leq s \leq s^*$). $Q_0$ might be given as a weighted average of two data items previously stored in $B_s$.

A MULTI-MICROPROCESSOR IMPLEMENTATION OF ARES

In order to effectively carry out the associative search on a semantic data base described in the previous sections, the following functions should be provided at the computer architecture level:

1. A hierarchical blurring capability.
2. The fundamental content-addressing capability.
3. A heuristic control mechanism to obtain a reasonable number of associated data items.

For the hierarchical blurring capability, a control logic is

Figure 3—Association through blurring and content-addressing

Figure 4—ARES main block diagram
necessary which offers an efficient access to the multiple blurred data spaces and executes the error correction schemes applied for the blurring. Binary cyclic codes are useful for a variety of applications because of the flexibility of selecting proper length and the easiness of implementing the error correction procedure.

As shown before in Figure 3, the content-addressing is accomplished in the blurred data space $B_s$ taking each blurring block of the final stage of blurring as a unit, and for all units in parallel. The number of blocks which coincide with each other is counted over all the blocks unmasked, and compared with a certain predefined threshold value $\theta$. When it is equal to or greater than $\theta$, the corresponding hit mark is set to 1, and the value of $\theta$ is gradually adjusted by the heuristic control mechanism embodied in ARES so that a greater number of associated data items as possible are obtained within the limit $\delta$.

In principle, these functions associated with the content-addressing can be accomplished by the mechanism which is incorporated in the uniprocessor ARES originally designed for the recognition of handwritten characters. However, in order to facilitate the blurring time after time and to effectively create the blurred data spaces, it is extremely desirable to provide a logic which works over many sets of blocks in data words simultaneously. Furthermore, a blurred data space should be spatially distributed again in order to execute the blurring and content-addressing for all data words in parallel. These concepts lead to a conclusion that a multiprocessor organization is the best of possible approaches to attain the advanced association facility described above.

**Architecture of ARES**

Figure 4 shows the block diagram of multiprocessor organization of ARES. The distributed processing requests the Master Control to synchronize the whole logic units. As the logic unit, a functionally flexible logic, for instance, a microprocessor (TI-SN74S481; 16Kbytes memory) is used since the data structure of semantic data bases might be considerably complicated depending upon the problems to be solved. Hereafter, the logic unit is referred to as a cell.

The Cluster Control controls eight cells all together, and the master control governs eight cluster controls. Therefore, up to eight different programs may be processed in eight different clusters of cells in parallel. On the other hand, in the case that all the cluster controls are assigned to process the same program, sixty-four parallel operations can be performed in the whole cells.

The Multiple Response Resolver (MRR) which is a unique facility in ARES is made up of a parallel counter with multiple inputs. Each MRR-1 receives the hit marks from the cells attached to it, and the contents of MRR-1’s are collected by MRR-2. The master control compares the content of MRR-2 with the predefined value of $\delta$ and adjusts the value of $\theta$ when necessary for further content-addressing. The design of MRR is basically made clear in Reference 4.

Figure 5 shows the internal structure of a cell which is the nucleus of the association logic. A data item and its blurred...
representations are accommodated in a cell together with the logic encountered in a conventional associative memory. The block size and the word size indicate the length of a blurring block at each stage of blurring and the length of a data item, respectively.

We may conclude that the clustering of cells supplies high reliability and functional flexibility; the loss of a single cell function or MRR-1 results in a slight decrease of processing power but no complete breakdown of the system, and each cluster of cells can perform its own function individually.

Functional behavior of ARES

The functional behavior of ARES for manipulating a semantic data base is explained as follows: The mini-computer HP-21MX is used as a Host Computer, and recognizes ARES as an associative memory with extremely high intelligence. The operation is initiated when the host computer issues a global command to the master control. The master control analyzes the command and gives the related subcommands to the cluster controls. This implies the function of pointing out the start addresses of the microprograms to be performed, which are previously stored in the cluster controls. Then each cluster control carries out the specified operation individually.

Figure 6 shows the relationship between the blurred data spaces and the corresponding cells in the blurring mode.

Each blurred data space is divided into subspaces and data items contained in a space are distributed to the cell memories so that they can be processed in parallel. The error correction for the blurring is accomplished through ALU shown in Figure 5, and controlled by the microprograms in the cluster control.

Figure 7 indicates the same relationship in the content-addressing mode. A query item and the value of $\delta$ are sent to each cell in parallel by the master control. The content-addressing is then performed in the blurred data space $B_{e^*}$, which are distributed in cell memories, with $\theta$ heuristically controlled by MRR under the parameter $\delta$. The control of $\theta$ is implemented in hardware because the very fast multiple associations are required repeatedly. The hardware is designed in consideration of the trade-off between the functional requirements imposed and the cost of implementation.

CONCLUSION

In this paper, the association principle presented before is extensively developed in order to be applied to the associative search on semantic data bases for speech or image understanding. Data items are coded in such a manner that the relatedness of the symbolic partial representations of segmental or categorical blocks of data items is measured in terms of the distance of the code vectors associated with them, and they are blurred by the hierarchical application of error correction schemes. Thus, by simply applying conventional content-addressing schemes to the blurred data items, the associative search of original data items is accomplished on their deep structured relatedness without executing the complex calculations of relatedness on original data representation.

Following the overview of the generalized association mechanism, we presented an architectural description of ARES which is now being developed. From the viewpoint of computer architecture, ARES has the following characteristic features: A multi-microprocessor organization is adopted using HP-21MX mini-computer and TI-SN74S481 Schottky PL bipolar microprocessors as a host computer and cell components, respectively. This provides both the structural extendibility and functional flexibility supported by microprogramming to adapt to a variety of applications in the field of artificial intelligence. Furthermore, ARES facilitates heuristic control of the number of associated data items, which is useful to solve pattern recognition problems.

So far we have discussed the associative search on semantic data bases for speech or image understanding. However, ARES can be well applied to natural language processing. For example, the associative-categorical model proposed by Haralick and Ripken for semantic word retrieving is dealt with by means of representing categorical relatedness of data items by code distances.

In conclusion, a multi-microprocessor ARES provides an advanced pattern recognition facility bridging the gap between human cognitive behavior and the logical processing by computers.
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REFERENCES


