

Charge-coupled devices for memory applications

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INTRODUCTION

Since the invention of charge-coupled devices (CCD) in late 1969,¹⁻³ the potential of the charge-coupling concept for digital memory has been recognized. Applications to image sensing and signal processing requirements have, however, preceded the application of CCD to memory. This occurred because relatively simple charge-coupled devices offered new performance potentials for image sensing and signal processing. Nonetheless, the basic shift-register nature of CCD implies that its greatest opportunity for widespread application lies in the highly competitive area of high density semiconductor memory. Today, sophisticated CCD memory components are emerging.

Although a CCD memory can be configured in a number of ways, all are basically serial in nature and, hence are block-access oriented rather than bit-access oriented. The charge-coupled device is characterized by high packing density, low power dissipation, and a structural elegance which will lead to very low cost. Besides being a natural semiconductor replacement for rotating drums, discs and other peripheral memories, CCD will ultimately find application in many main-frame requirements as systems architecture evolves to take advantage of these fast, lower cost block-oriented components.

This paper begins by describing the general properties of CCD memories, focusing on speed, power, temperature characteristics, and interface requirements. Next described are three basic classes of CCD memory components—the Synchronous, the Series-Parallel-Series, and the Line Addressable. As a specific example, a Synchronous configuration with 9216 bits and fabricated with Isoplanar, buried channel processing is described in detail.

GENERAL PROPERTIES OF CCD MEMORIES

Speed

The movement of charge from one CCD electrode to the next is inherently fast, ultimately limited only by the carrier saturation velocity. Registers which shift data effi-

ciently at frequencies in excess of 100MHz have been reported by Esser.⁴ Improvement by factors of 2 or 3 over these values is only a matter of time. Such speeds will not be as easily achieved in useful CCD memory components. In a practical memory component, significant peripheral and interface circuits are required. These include read/write logic, level converters, sense amplifiers, and I/O buffers. In current practice these circuits are implemented, as is the CCD, by N-channel MOS technology. For standard voltages and present design rules, such circuits are limited to about 10MHz with 5 to 7MHz representing a more practical current upper limit for production devices.

Power dissipation

The dynamic, non-equilibrium operating mode of the CCD element leads to an almost ideal energy transfer condition where on-chip power dissipation is associated primarily with the movement of signal charge (data). If, on the average, one-half the bit sites contain charge, the speed-power product for typical parameters is 0.2pJ per bit transferred. As an illustration, consider a simple series shift register block of N bits. The average power dissipated on-chip for a data frequency of f_c is given by:

$$P = 2N(0.2 \times 10^{-12})f_c. \quad (1)$$

If $N = 1024$ and $f_c = 5\text{MHz}$, then

$$P = 2mW \quad (2)$$

which is a small power for a memory of this size. Moreover, in other configurations where most of the data is moving slowly or not at all, the power per bit is averaged downward very much further.

A much more significant term is the power dissipated in the drivers to the CCD register. Since the CCD electrodes present a substantial capacitive load, the drivers dissipate power according to the general law for reactive power,

$$P = CV^2f_c$$

For the simple series shift register considered above, the capacitance per bit for an Isoplanar, buried channel structure is approximately $C_b = 60fF$. For $V = 10V$ and

$f_c = 5\text{MHz}$, the driver power becomes

$$P = 2NC_b V^2 f_c = 60\text{mW} \quad (3)$$

Although this is much larger than the real power dissipated in the CCD, it is quite acceptable. The driver power requirement can be averaged downward by slowing the clock frequency when the memory is not actively used.

Perhaps the largest on-chip power dissipation is in the peripheral circuitry. Although it is difficult to be quantitative without a particular memory configuration in mind, a power dissipation of one to two orders of magnitude higher than the CCD storage elements can be expected.

Temperature behavior

The CCD storage element is dynamic and therefore, must be periodically refreshed similarly to a dynamic MOS RAM. The frequency of refresh is a sensitive function of temperature. At room temperature (25°C), the element storage time is of the order of one second. This value decreases by a factor of two for every 9°C increase in temperature up to approximately 70°C . Above this it decreases even more rapidly, until at 125°C , it is falling a factor of two every 4.5°C . For an ambient temperature of 70°C , a typical die temperature might be around 90°C . Since under these conditions the storage time is approximately 5ms, the memory must be refreshed more frequently than at lower temperatures. This increase in refresh rate increases power dissipation which, in turn, increases the difference between the ambient temperature and the die temperature thereby further increasing the required refresh rate. The power dissipation, therefore, increases in a power law fashion as the system ambient temperature rises. Conversely, at artificially lowered temperatures ($<25^\circ\text{C}$) the power and time required for refresh rapidly becomes insignificant. For example, at -30°C ambient, the storage time is approximately one-third of a minute which thereby renders the memory close to non-volatile from a power dissipation standpoint. Future memory systems using CCD may find it advantageous in many instances to incorporate cooling for increased system performance.

Interfacing and packaging

As a result of the extensive use of NMOS technology for the on-chip peripheral circuits, CCD memory components should be no more difficult to use than dynamic MOS circuits. Indeed, dependent on design, the timing and other requirements may be superior to MOS.

The similarity of CCD memory to MOS memory will lead to the use of essentially identical packaging technology, which includes side-brazed ceramic, cerdip and plastic. The designing and qualification cycles should be rapid.

MEMORY CONFIGURATIONS

The inherent digital CCD configuration is that of a shift register with a serial-in/serial out operation where all bits are simultaneously shifted. CCD memory elements can be formed by using these shift registers directly or by combining the shift registers with refresh, sense and decoding circuitry to construct more sophisticated memory chips. There are three basic organizations for memory applications:

(1) Synchronous

The synchronous organization is one in which all shift register segments are clocked simultaneously. For example, the well-known serpentine configuration is synchronous. This organization (Figure 1a) is obtained by connecting in tandem several sequential multi-stage shift registers by means of refresh cells. Internally, all data bits are simultaneously shifted through all cells of the register and characteristic of the synchronous organizations, the internal shift frequency is equal to the input/output data rate. An important advantage of the serpentine configuration is that it permits the construction of extremely long shift registers with excellent low frequency response even at elevated temperatures where leakage currents become significant. A disadvantage of this organization is that power dissipation is higher at a given operating frequency than the other approaches because all bits of data are moving at the same frequency. Additionally, the clock power requirements are high for a large capacity memory since the clock-line capacitance is relatively high. Several serpentine shift registers can be combined on a single chip using common control signals and an address decoder which enables selection of one or more of the serpentine registers. Because all of the serpentine memory operates at the same frequency, it can operate over a wide range of frequencies, which is particularly useful for data buffering applications.

(2) Serial-Parallel-Serial (SPS)

The power efficiency and effective packing density of the basic CCD shift register can be increased by performing a serial-parallel-serial (SPS) manipulation of the data. An SPS memory arrangement is shown schematically in Figure 1b. The input rate is determined by the clock frequency of the horizontal registers. After filling the top horizontal register with data, a parallel operation is performed in which all of this information is shifted into the vertical registers. Thus, the vertical registers run at a frequency equal to N^{-1} of that of the horizontal registers where N is the number of bits in the horizontal register. If it is assumed that the total number of bits is $N \times M$, the delay from input to output is NM/f_h where f_h is the horizontal clock frequency. However, the number of stages of shift register through which any one bit is transferred equals only $N+M$.

One advantage of this configuration is that the power dissipation is low because most of the data bits are moving at the slow (vertical) clock rate. This reduction in power dissipation is obtained at the expense of an additional set

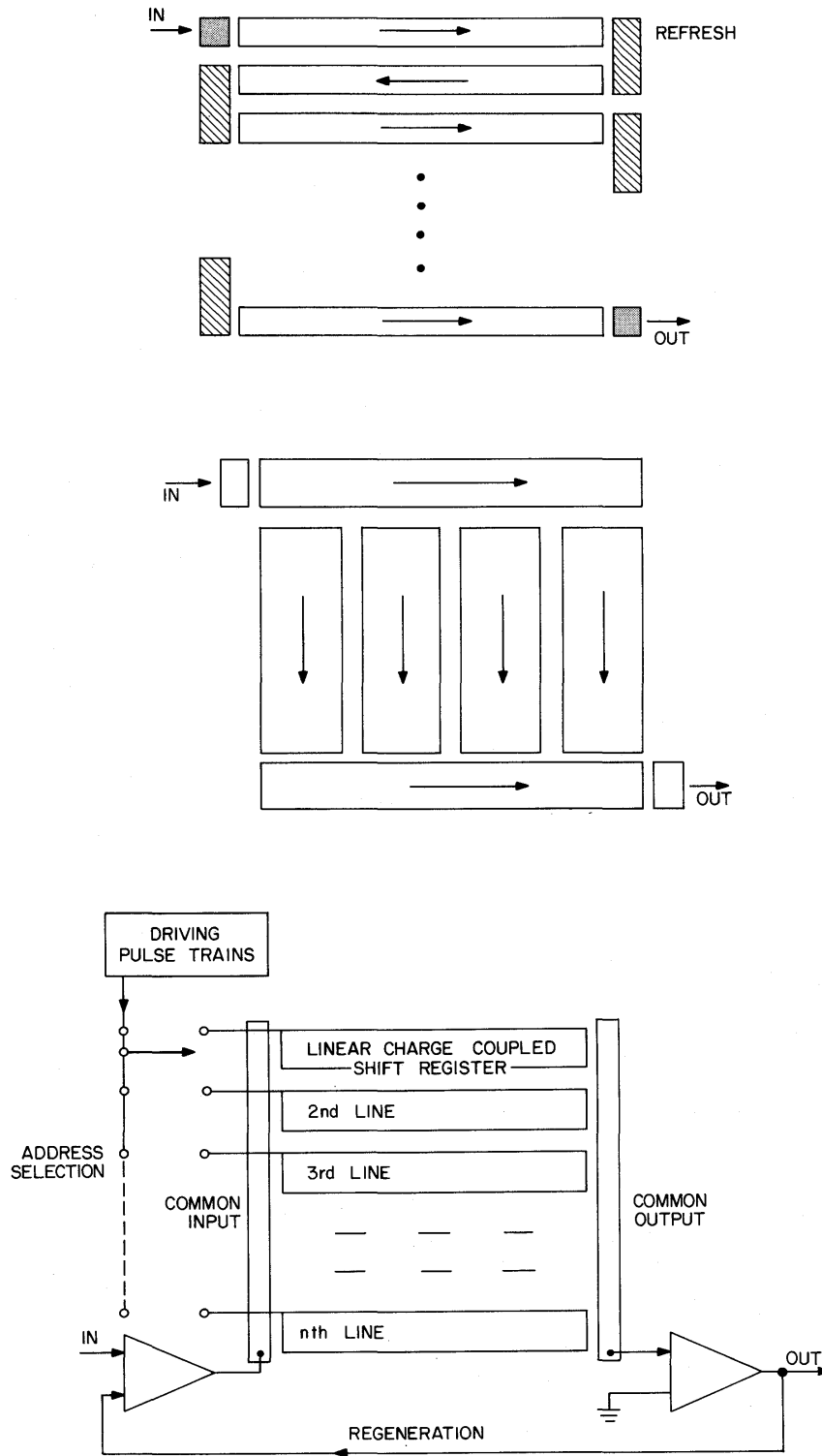


Figure 1—A schematic representation of a charge-coupled. (a) serpentine shift register organization. (b) serial-parallel-serial (SPS) shift register organization. (c) line addressable random access memory (LARAM) organization

TABLE I

Memory Class	Application	CCD Memory Order of Preference
FAST ACCESS MEMORY	(Fast Access Bulk Storage	LARAM
	(Main Memory Mini CPU	Synchronous
	(Signal Processing	SPS
	(Multistation Data Collection	
	(Disc Enhancement	
SERIAL MEMORY	(Airborne Mag Tape Repl.	
	(Commercial Disc	SPS
	(Commercial Tape	LARAM
	(Lightweight Field Data Collection	Synchronous
	(Communications Buffers, Large Record	
BUFFER MEMORY	(Multiplex Communications Buffers	Synchronous
	(Buffered I/O controllers	SPS LARAM

of clocks for the vertical registers. Another advantage is flexibility in timing if the vertical clocks are programmable. Additional flexibility can be achieved with separate input and output clocking.

A disadvantage is the long delay between input and output. This limits the low frequency and high temperature operation of the memory, because of leakage currents. Similarly, the access times for SPS memory chips are generally longer than those for other organizations. It should be noted, however, that the data rate can still be very high. Overall, the SPS characteristics make it very attractive as a potential replacement for mechanical memories.

(3) Line-Addressable

Although a true random bit-access capability is inherently precluded by the very nature of the CCD storage structure, a novel organization has been conceived which does provide a pseudo-random access with access times in the tens of microseconds. This is the line-addressable random access memory (LARAM) configuration which is an integration of CCD and MOS memory concepts. One form of the LARAM is illustrated in a simplified schematic form in Figure 1c. Basically, the memory is composed of an MOS address selection matrix and a number of CCD sequential shift registers, where each register represents a line. Selection of an address causes the driving waveforms to be applied to the chosen line (register) to initiate read-out/write-in/ or refresh or information in that register.

This configuration allows an access time that is essentially dependent on the number of elements per line. In addition, since only one line is operative at any one time, clock capacitance and power dissipation are minimal. Dependent on the stack configuration, a memory system using a line-addressable structure can be either word-organized, where each line represents one or more words, or bit-organized, where each line contains one

particular bit of a number of words. Since the data is, in general, not moving most of the time, this type of device organization has the most stringent requirement on dark current uniformity. Nonetheless, this organization is the most flexible and will find greatest application in cache buffers, swapping stores and mainframes.

Other organizations which are basically derivatives of those above include among others, the multiplexed electrode-per-bit⁵ configuration, the interlaced SPS⁶ and the addressed drum type structure.⁷

In the multiplexed electrode per bit configuration each *electrode* is used as a storage site. The clocking is such that only 1 of N electrodes is clocked at a time thus propagating a "hole" through the stored data. For the price of an N -phase clock ($N \gg 1$) the packing density of the memory can be doubled. The interlaced SPS is just like any other SPS except there is one horizontal electrode rather than one bit for each vertical register. Clocking is such that the odd and even vertical registers are alternately filled from the odd and even electrodes of the horizontal input register. At the output, this sequence is pursued in an analogous but reverse manner. The addressed drum type structure is a synchronous organization similar to the serpentine configuration except each loop closes back on itself. Access to these independent loops is by means of an address decode for the I/O.

Several organizations will emerge as standard CCD memory products as a result of the complex trade-offs between system requirements and device economies. A qualitative comparison of the three basic organizations for different applications is shown in Table I. Note that in the critical area of fast access memories (FAM's), the LARAM is the preferred configuration. This choice derives from the fast access time and low clock capacitance characteristic of this organization which permits easy memory expansion. In addition, the power dissipation is low and the organization leads naturally to a high density layout. As a result of these unique features, the LARAM will play a major role in the application of CCD to system design and layout. For serial memory, the SPS is preferred because of its simplicity. Finally, for buffer memory synchronous architecture is preferred because of its versatility and ease of use.

EXPERIMENTAL RESULTS

In order to put the above remarks in a realistic frame of reference, this section deals with a specific CCD/NMOS

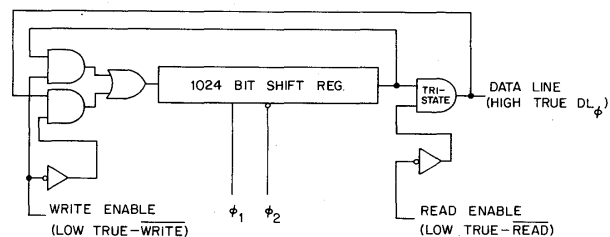


Figure 2—A logic diagram for one of the nine channels in the CCD450

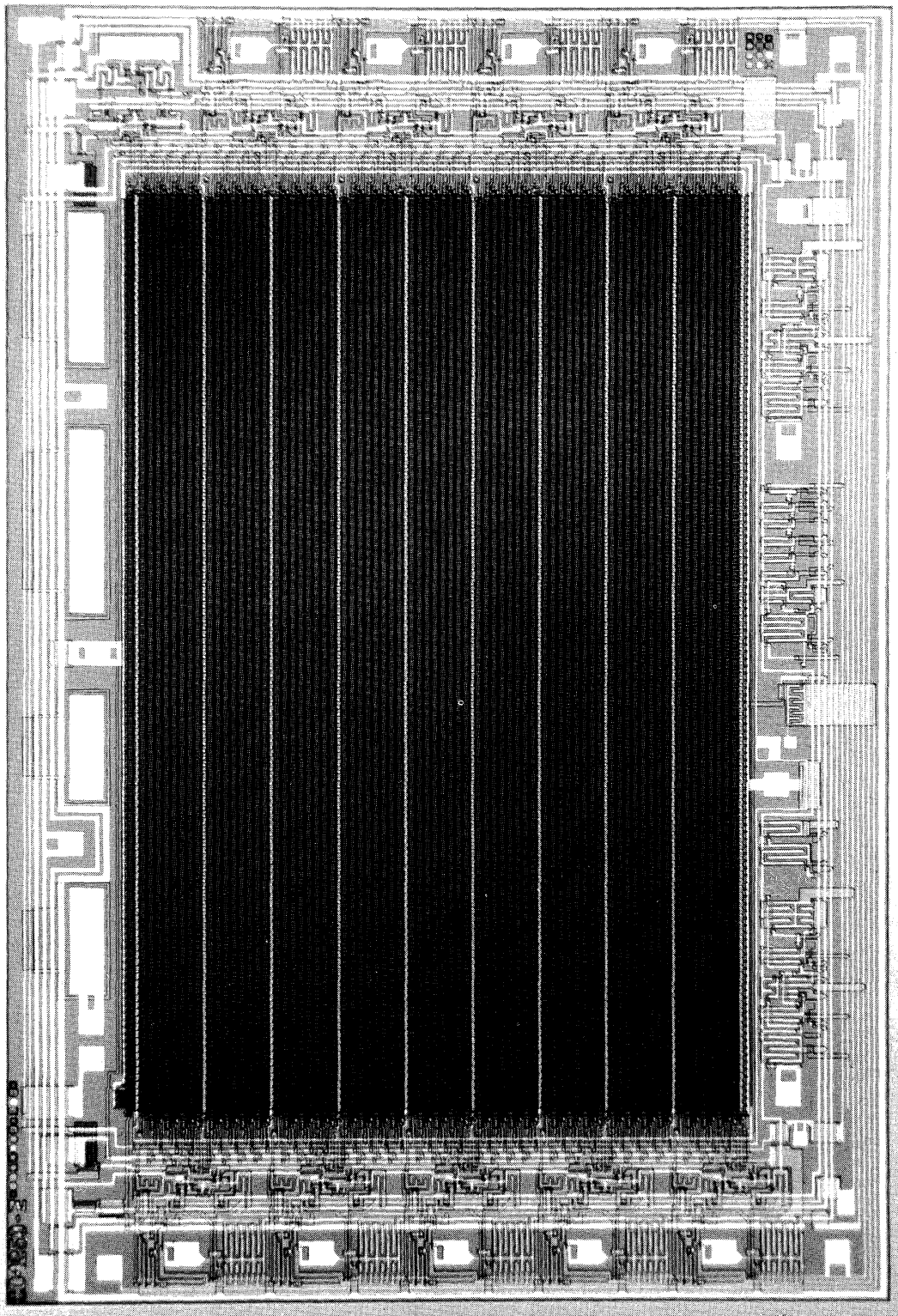
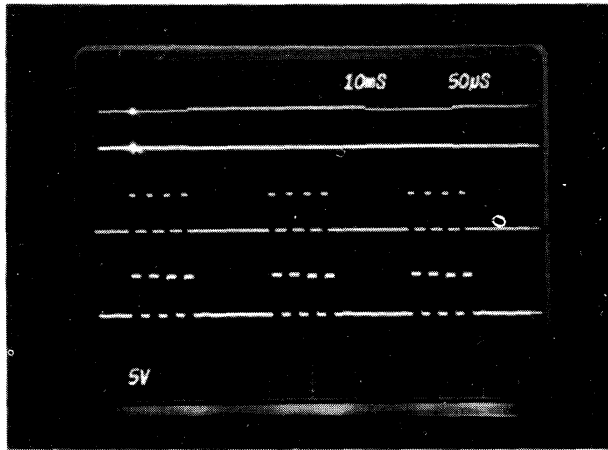
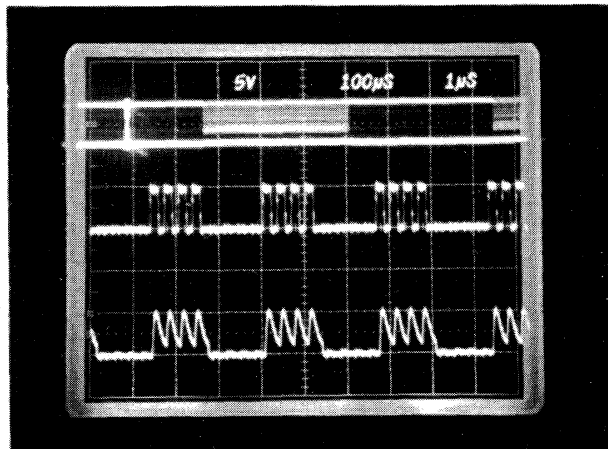


Figure 3—Photomicrograph of the CCD450



(a) 50 KHz Data Rate



(b) 3MHz Data Rate

Figure 4—Oscilloscope traces of one channel of CCD450 operating at 50KHz and at 3MHz. The lower two traces show input data and output data respectively

memory component which has been developed at Fairchild. This part is known as the CCD450.

Description

The CCD450 is a serial storage memory consisting of 9216 bits which are organized into a format of 1024 bytes by 9 bits. This architecture is realized by the use of nine shift registers each containing 1024 bits. Since these registers are shifted in parallel, nine-bit bytes are stored or retrieved in a byte-serial mode.

The component represents a significant advance in semiconductor memory. Although it contains all the logic necessary to facilitate ease of use the average density is less than 3 mil²/bit. The fabrication of the memory is little more complicated than comparable *N*-channel MOS circuits with only one additional photomasking operation. On-chip TTL-to-MOS level conversion permits all logic and data lines to be TTL compatible. On-chip timing reduces the system requirements to simple two phase clocks. Bi-directional tri-state data lines and commonality of logic for I/O control permit the memory to be packaged in a 0.3 inch 18 pin standard package.

A logic diagram for one of the nine registers is shown in Figure 2. Each register is accessed by its own bi-directional data line, but all nine registers are serviced by common data-transfer clocks (ϕ_1 and ϕ_2) and control functions READ and WRITE. Not shown on the logic diagram, but also common, are the DC power supply lines and a data-enable (DE) line. The data lines are driven with a tri-state buffer, thus providing a "wired OR" capability at the output. This eases memory system expansion, eliminating the need for interfacing components on the PC board.

The CCD registers are organized in a serpentine fashion with refresh turn-around-cells every 128 bits. The CCD structure used is a buried channel, gapless structure with ion-implanted barriers. The MOS circuits used to provide timing, charge detection and level conversion are fabricated using Fairchild's n-channel silicon gate Isoplanar^(R) process. Figure 3 is a photograph of the chip.

Performance

The operating modes of the circuit include: read, write, read/modify/write, and recirculate. Furthermore, depending upon the data transfer rate, the recirculate mode can be broken down into a search mode and a standby mode.

The basic timing is established by the two clocks (ϕ_1 and ϕ_2). During ϕ_1 high time, the logic is reset, data is shifted by $\frac{1}{2}$ bit and the mode control level conversion from TTL to MOS levels is accomplished. During ϕ_2 high time the data is shifted by $\frac{1}{2}$ bit, output charge (or lack of charge) is sensed and presented to the output and, simultaneously, is written into the first CCD stage. The charge level written into the first CCD well is controlled either by the output charge level or the data pin state depending upon whether the selected mode is *recirculate* or *write*. Figure 4 shows

TABLE II—Summary of CCD450 Characteristics

ORGANIZATION:	1024 BITS x 9 BITS
OPERATING FREQUENCY:	3 MHz MAX READ, WRITE OR RECIRCULATE 2 MHz MAX READ/MODIFY/WRITE 50 KHz MIN STANDBY
INPUT/OUTPUT INTERFACE:	TTL COMPATIBLE BI-DIRECTIONAL DATA BUS
READ/WRITE LOGIC INTERFACE:	TTL COMPATIBLE "LOW-TRUE" LOGIC INPUTS
CCD CLOCKS:	TWO-PHASE CLOCKS (ϕ_1 AND ϕ_2)
DATA ENABLE CONTROL:	DISABLES READ/WRITE BUFFER FOR LOW POWER STANDBY OPERATION (0-12 VOLTS)
POWER DISSIPATION:	READ—AT 3 MHz—250 mW TYP. RECIRCULATE AT 3 MHz—50 mW TYP. STANDBY AT 50 KHz—30 mW TYP.
CLOCK CAPACITANCE:	400 pF MAX.
VOLTAGE REQUIREMENTS:	ϕ_1, ϕ_2 AND DE 0-12V CLOCKS V_{DD} +12 Vdc V_{CC} +5 Vdc
PACKAGE:	18-LEAD D.I.P. (300 MIL WIDTH)

one channel of the memory operating in a write/recirculate/read mode at 50KHz and at 3 MHz.

During the recirculate mode, only those circuits required for internal data transfer need to be active. This selection is accomplished by bringing the data enable (DE) line to its low state, thus disabling the read and write logic. While in this state, the chip will disregard the READ and WRITE lines, thus removing all constraints on these lines during the recirculate mode. This mode is thus useful for either a high speed "search" operation, or a low speed, low power standby operation.

A low power standby mode can be obtained by reducing the operating frequency. Further power reductions can be obtained by reducing the duty cycle, operating with both ϕ_1 and ϕ_2 low for much of the cycle. Table II lists the device characteristics.

Application

The CCD450 is most conveniently envisioned as a byte-organized dynamic shift register with sufficient overhead functions to ease its use considerably. As such, it is most attractive for terminal applications where the byte organization and low power are highly desirable. In this application, it replaces more than nine packages, saves several square inches of board space and reduces power dissipation by more than an order of magnitude. The low power recirculate mode permits battery back-up for non-volatility and portability.

CONCLUSIONS

The charge-coupled device will play a major role in future semiconductor memory systems. Its characteristics of low complexity, low power dissipation, high data rate and ease of use will result in rapid growth in numerous memory applications and produce concomitant reduction in cost/bit.

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