High speed modular multiplier and digital filter for LSI development

by DON F. CALHOUN
Hughes Aircraft Company
Culver City, California

INTRODUCTION
In order to realize the increased economy and reliability of systems implemented in large chip or full wafer LSI, five requirements must be satisfied:

1. Systems must be organized and partitioned to obtain a high gate-to-logic pin ratio in order to maximize the use of wafer components.
2. Efficient use must be made of standard logic cells more complex than current IC chips.
3. Logic cells must be defined to both facilitate automated routing and to allow automated testing with a restricted number of test points.
4. Discretionary interconnect of logic elements must be eliminated or minimized.
5. Sufficient redundancy must be used to ensure reliability, facilitate testing, and allow economical interconnect in view of non-100 percent yields.

An efficient and original scheme for modularizing a general purpose high speed digital filter is described in this paper. The prime components of this filter are the Modular Carry Advance Multiplier and Adder which meet the first three requirements above extremely well. In a future paper, a technique will be presented which offers a unique means of economically obtaining a specified standard pattern of good circuits on either an LSI chip or an entire wafer. The use of this technique for LSI non-discretionary signal routing helps to meet requirements (4) and (5) by standardizing all signal interconnect and facilitating automated testing.

High speed modular multiplication for LSI development

The Modular Carry Advance Multiplier uses an original algorithm and implementation to provide very high speed multiplication for any wordlength operands. The technique is most important to any digital processing requirement such as Fast Fourier transforms, pulse compression, digital filtering, or even general purpose computers which require very high speed multiplication. The highly efficient modular logic characteristics and the use of a single circuit type (i.e., a gated full adder, NAND gate, or NOR gate) make it a system very applicable to efficient LSI implementation. Thus, the Modular Multiplier is both an excellent vehicle for the development of LSI processing, testing, and packaging technologies, and is, in itself, an important instrument with which to meet the current and future high speed digital processing requirements.

Emphasis in the description of the multiplier is placed on the modular design techniques which provide the very important characteristics for LSI development of efficient standard modules that: (1) obtain a very high gate-to-pin ratio of 43 for an 8-bit multiplication, (2) require only one circuit type, (3) are readily diagnosable, and (4) allow a one-time logic design that does not require temporary storage, control, or shift logic for any wordlength. Finally, the organization of an entire digital filter is described which meets the LSI
criteria and uses the Modular Multiplier as the key component in its high speed design.

Design of the modular carry advance multiplier

There are two original concepts in the design of the Modular Carry Advance Multiplier. First, the most general multiplication technique of summing the columns of a matrix formed by ANDing and shifting the multiplier-multiplicand bit pairs (as shown in Figure 1 for an 8-bit multiplication) has been analyzed to determine independent and modular blocks of logic which allow partial products to be determined in parallel and then summed to form the final product. The most efficient division of the multiplication matrix into modular logic blocks is accomplished by forming geometrically similar blocks within the matrix as shown by the dashed lines where an 8-bit multiplication is partitioned into four identical 4-bit multiplier blocks (MB1-MB4). Since these four logic blocks are independent, each can function in parallel to determine 8-bit partial products by the column summation of the bits in its portion of the large products in a three-input adder is the final product.

Since the four segments of the multiplication matrix are reduced at once and since the multiplication matrix itself has pre-determined the shifts required, no control, temporary storage, or shift logic is required. By this simplification of the column summations into shorter, parallel operations without control logic, a significant speed advantage is obtained. In addition, a modular multiplier block has been defined which can be used to build any longer wordlength multiplication by paralleling modules and summing their outputs.

The bit length of the multiplier module can be determined by the yields of different complexity LSI chips and by the efficiency obtained for various multiplication wordlengths. In any case, the modular multiplier reduces the maximum multiplication delay from N full wordlength additions and shifts for the classical one-bit-at-a-time technique to that of only one double-wordlength addition. Since most of this delay occurs in the adder which sums the partial products, look-ahead or other speed-up techniques in the adder will further improve the speed beyond that reported herein.

The second original technique in the modular multiplier is the asynchronous carry advance philosophy that is used to implement with a single circuit type the multi-operand addition required both in the multiplier modules and in the final adder. The carry advance implementation performs the simultaneous addition of multiple operands with any carries being asynchronously advanced toward the output rather than being "saved" or propagated in a ripple-carry fashion. The logic signals with the shortest delay paths are reduced first, thus adding less delay to the most critical paths.

In general, if K-bit modular building blocks are used, \((N/K)^2\) of the blocks allow the multiplication of two N-bit (magnitude) operands, where N is unrestricted. These operate in parallel to form partial products which are then reduced to the final product by a \((2N-K)\) bit adder. In general, an \((N\ by\ N)\) bit multiplication with register storage of the product will require 6 SUM and \((2N-3)\) CARRY delays. A hybrid chip-and-wire MSI multiplier module (Figure 2) and an integrated circuit breadboard (Figure 3) which form 8-bit products have been built and tested (see Figure 4) show a 12-MHz multiplication rate using 12 of the relatively slow SN5480 gated full adders. The hybrid MSI multiplier was fabricated on a 1-inch square ceramic substrate. The introduction of a 6-bit latch register would allow the 12-MHz rate to be nearly doubled via pipelining.

As an example of paralleling identical multiplier blocks to build longer wordlength multiplications, consider the multiplication of two 8-bit operands as shown in Figure 5. As for the general case in Figure 1, the four 4-bit multipliers (MB1-MB4) are defined by forming the smaller, geometrically similar matrices, each of which determines the product of four of the multiplier bits.

---

**FIGURE 1—Four modular 4-bit multipliers for the multiplication of two 8-bit operands**

---

From the collection of the Computer History Museum (www.computerhistory.org)
and four of the multiplicand bits. Figure 6 shows the independent operation of MB1 through MB4 to determine in parallel the 8-bit partial products PP1 through PP4, respectively. Because PP1-PP4 have different magnitude effects on the final product, the outputs of MB1-MB4 are staggered when input to the adder whose inputs are shown in Figure 7. Because the partial products are stag-
Figure 7—Adder inputs for multiplication of Figure 6

generated in this fashion, the adder need only be a three-input 12-bit adder in order to determine a 16-bit product. This can be reduced to a 10-bit delay by doing a simple look-ahead in the last three bits which does not require additional circuits if gated full adders are used. And, since the multiplier block delay is equivalent to a 6-bit addition, the longest delay to multiply two 8-bit numbers is equivalent to a double wordlength (i.e., 16-bit) addition.

Figure 8 shows the logic required in each of the identical 4-bit multiplier blocks with the inputs being ANDed multiplier-multiplicand bits if non-gated full adders are used. The longest delay is from the SUM (S) output of the first FA3 or from the CARRY (C) output of FA2 to the S output of FA7. If gated full adders are used as the logic blocks, only the four multiplier and four multiplicand bits are necessary at the left as inputs. That is, the gated full adders can generate the required "AND" of the multiplier-multiplicand bit pairs as well as determine the SUM and CARRY outputs. Otherwise, the ANDing function of the multiplier-multiplicand bit pairs must be generated external to the full adder blocks. The design that has been breadboarded and tested requires only 12 SN5480 gated full adders per 4-bit multiplier block. Thus, to multiply two 8-bit operands, 48 full adders are needed for the modular multiplier blocks, 19 for the adder, 1 as a sign determining circuit, and 34 gated full adders to implement a 17-bit product register. This totals only 102 gated full adder circuits and is well within the goals of full-wafer LSI technology. Only 38 external connections are required which obtains a very high gate to pin ratio of 43 since each gated full adder is logically equivalent to 16 two-input NAND gates. If 16 additional input pins and 12 full adder circuits are added, a 16-bit number can be added to the product which represents all the arithmetic processing necessary to accumulate the finite sum of products required in linear digital filtering.

Use of an "Integrated Electronic Component" as the basic logic block

All logic functions in the multiplier, adder, and register can be accomplished with NAND gates, NOR gates, or with gated full adders (e.g., the Texas Instruments SN5480 "Integrated Electronic Component"). This gated full adder chip (shown logically in Figure 9) is used efficiently in different modes to obtain the functions of a full adder, half adder, NAND gate, single-input inverter, and flip-flop (by cross-coupling the input gates). In addition, conversion to one’s or two’s complement notation can be accomplished in the adder by appropriate use of full adder input gates. The use of this single circuit type as a logic building block and the modular characteristics of the multiplier are especially important since they provide a sys-

FIGURE 8—Design of 4-bit carry advance multiplier

FIGURE 9—SN 5480 full adder with gating and interconnection pads shown
tem very applicable to LSI development which can greatly reduce the cost and volume per circuit of this high-speed design. A further advantage to choosing a gated full adder as the single circuit type is that its logic is equivalent to 16 preconnected NAND gates that greatly reduce the number of circuit chips and interconnections required between circuits. The simplification of interconnect by using more complex logic chips as building blocks in an LSI implementation is especially important.

The design of the modular multiplier with the product register is about 85 percent as efficient (in number of IC chips) as an optimum design using gates and full adders, but at that high an efficiency it is far more desirable for LSI processing techniques than a mixed circuit design since it offers extreme advantages in both the wafer processing and circuit interconnect. Furthermore, the area of an SN5480 circuit is 3600 mil$^2$ for 16 gates while the area of an SN5400 quad two-input NAND gate is 3000 mil$^2$. Thus, the SN5480 has 333 percent more circuits per area than the SN 5400 quad two-input NAND gates. For any application that makes much use of full adder functions, such as the design presented here, a gated full adder is seen to be a much more efficient circuit type. Because it is a complete logic building block and offers the great logic flexibility described above, it may be found to be quite important for other LSI systems.

**Summary of modular carry advance multiplication characteristics**

The Modular Carry Advance Multiplier has been described having the following characteristics:

1. An efficient, high speed design (30 MHz with MECL II for 8-bit products) is used. For example, a four-times speed increase is obtained over two-bit-at-a-time ternary multiplication using a look-ahead adder.
2. The modular multiplier is implemented with a single circuit type (a gated full adder) of high logic capability which minimizes the unit volume and interconnection.
3. The modular logic design allows any word-length multiplication to be built by paralleling more identical building blocks.
4. No control, shift, or storage logic is required, thus permitting a maximum gate-to-pin ratio (43 for an 8-bit multiplier).
5. The multiplier is easily tested from inputs and outputs alone by using counters for the inputs and monitoring the outputs of two or more units with a simple comparator. Total test time for entire 1600 gate wafers is about 200 $\mu$s.
6. By using $Q$ additional full adders, a $Q$-bit operand can be added to the product while it is being formed with only one additional SUM delay. That is, $(A \times B) + P$ could be generated with only one additional SUM delay beyond the time required to generate $(A \times B)$. This has a most important application in radar data processing as described later since it entails all the arithmetic processing required in digital filtering, pulse compression, or correlation calculations.
7. Pipelining of a Modular Carry Advance Multiplier can be used to both gain speed and save circuits in long wordlength applications. That is, successive groups of the multiplier and multiplicand bits can be sequenced through a single modular multiplier which forms a partial product that is summed with the sum of previous partial products until all multiplier-multiplicand groups have been multiplied. For example, Figure 10 shows the multiplication of two 32-bit operands by sequencing 8-bit groups of the multiplier and multiplicand through the multiplier 16 times. Thus, sixteen 12-bit additions are required and at 20 ns per stage, $(16 \times 12 \times 20) \text{ ns} = 3.84 \mu s$ is the total delay to form the 64-bit product.
8. The combination of efficient modularity, very high gate to pin ratio, and the fault

![FIGURE 10—Multiplication of two 32-bit operands by sequencing 8-bit groups of multiplier and multiplicand through multiplier 16 times](From the collection of the Computer History Museum (www.computerhistory.org))
isolation characteristics allow the Modular Carry Advance Multiplier to obtain the increased reliability and economy of LSI implementation.

Automated diagnosis of an LSI modular multiplier and digital filter

The 8-bit plus sign modular multiplier that has been discussed consists of four 4-bit multiplier modules, a 12-bit adder, and a 17-bit product register. The adder and register can be combined into one 4-bit module type allowing four of these 4-bit modules to perform the partial product addition and storage. Thus, two modular unit types can be defined on an LSI wafer which together comprise the multiplier that develops a 17-bit sign and magnitude product. If the partial products developed by the multiplier blocks are available at test points external to the wafer, access can then be gained to each of the eight modules to test and isolate any failure to a single module. Since only combinatorial logic is used, and there are only $2^8$ combinations of inputs to each module, complete, exhaustive testing of the modules is both fast and straightforward. Figure 11 shows the simple test-bed of two 4-bit counters, two 8-bit registers, and an 8-bit comparator that can be used to automatically test the modules of two LSI wafers exhaustively. Each successful comparison clocks the multiplier to its next state and a multiplier carry-out clocks the multiplicand into its next state, thus successively generating all $2^8$ combinations of inputs. If a comparison is not made, the FAIL signal is given and the counters are left in their last state so that a logical diagnosis can, if desired, isolate the fault to one of the 12 to 14 full adders in the bad module. This simple automated test procedure can proceed at speeds of 200 $\mu$s per LSI wafer. Because the Modular Multiplier allows an LSI wafer to be efficiently partitioned into smaller cells that can be readily diagnosed, it is an excellent vehicle with which to develop the full wafer LSI technology with multi-layer interconnect. A fully automated test bed for 4-bit multiplier modules fabricated on a single LSI wafer chip is currently being built at Hughes. Figure 12 shows, in the bordered regions, three of these 4-bit multiplier chips on a 1½-inch wafer of SN5480 circuits. The twelve circled circuits within each bordered area specify the gated full adders that will be interconnected with two levels of metal to implement the multiplication. These 4-bit multipliers of 200 gate complexity having a quarter of a square inch of wafer area will be separately tested and packaged to provide an important step toward processing a full wafer of 1600 gate complexity that will develop and store in a register a 17-bit product.

FIGURE 11—Simple test-bed of two 4-bit counters, two 8-bit registers, and 8-bit comparator for automatic testing of modules of two LSI wafers

FIGURE 12—Three half-inch square chips of SN 5480's that will be interconnected and packaged as 4-bit modular multipliers
Slight modification of the testing approach will allow the exhaustive testing of an entire digital filter. Figure 13 shows how two registers (A and B) can simulate the input data and two computers (labeled SINE and COSINE) can be used to generate successively the phasor multiplier coefficients for A and B. By clocking the SINE and COSINE counters and the shift register memory, the successive outputs of the shift register can be compared with the expected results until a failure is detected or all the phasor multipliers have been used. In the latter case, another set of A and B inputs can then be used for another test sequence. Since these tests can be made as a free-running and self-stopping comparison (as described for Figure 11), the total exhaustive digital filter test time will be only a few seconds or less.

**A high-speed general-purpose digital filter of modular design**

As already described, the Modular Carry Advance Multiplier can readily be expanded in word-length by paralleling more of the modular multiplier-adder blocks. The total multiplication delay remains equal to the addition time of two numbers the length of the product, and the multiplication rate can be set simply by the rate at which the product is clocked from the multiplier (up to the maximum multiply rate as determined by the particular circuit type used). The preceding Summary mentioned how, in addition to forming the product of \((A \times B)\), another number could very efficiently be added to this product to form \(((A \times B) + P)\). This unique capability to accumulate a sum of products in a highly efficient modular and expandable fashion is most important to the design of digital filter banks which can readily be configured from these standard modules to meet the processing requirements of a wide range of systems.

As an example application, consider a radar filter bank having 16 filters and 32 8-bit pulse returns per filter dump. Figure 14 uses an unbuffered filter bank as an example of how the real and imaginary components of each pulse return can be multiplied by the appropriate filter phase shifts using the modular multiplier blocks. The partial products formed are summed with the previous sum of products for that filter by adding an additional input to the carry advance adder and bringing the previous sum to the adder from a shift register memory. Thus, the adder output is

\[
P_i^k = ((A_i \times B_i^k) + P_{i-1}^k)
\] (1)

**FIGURE 13—Diagnosis of entire digital filter**

**FIGURE 14—Unbuffered digital filter implemented with standard multiplier, adder, and shift register modules**
The use of the Modular Carry Advance technique to form sums of products as required in a wide range of digital filtering applications uses, at most, three types of standard modules which can efficiently be configured to satisfy the widely varying requirements of different systems. The same modules are as efficient in systems whose wordlength, input pulse or data rate, number of filters, and number of range bins vary significantly. The three modules that are used to meet these various system requirements are the Modular 4-bit Multiplier, the Carry Advance Adder, and the High-Speed Shift Register. The Modular 4-bit Multiplier and the multi-operand Carry Advance Addition technique have been described in detail above. The Carry Advance Adder modules, however, may be modified with look-ahead logic for higher speed and with additional inputs to allow for expansion in wordlength with minimum system modification. The shift register modules will be 4, 8, or 16-bit serial increments compatible to the processor logic and allowing simple modification in wordlength and/or number of filters.

A wide range of processing rates is determined by various circuit implementations of the Multiplier-Adder modules shown in Table II. If very high speed processing is required, the High Speed Modular Filter implemented with high speed circuits (e.g., MECL II or III) and using look-ahead addition with latch registers for pipelining can provide complex multiplication rates in excess of 30 MHz for forming 17-bit sign-and-magnitude products. This would be most important for applications requiring high data pulse rates or a large number of range bins or filters. If these requirements did not exist, a 6 MHz complex multiply rate (equivalent to a 24 MHz “simple” multiply rate) could be obtained by doing serially the four simple multiplies required in a complex multiplication. This use of a single set of modular multiplier blocks (rather than four sets) would allow the package count to drop by at least two to one. The modular filter design allows this clear trade-off between number of modules and processing speed while requiring no new module types when modification is necessary in the wordlength or processing speed (i.e., data pulse rate, number of range bins, or number of filters). Only the Modular Carry Advance Multiplier-Adder algorithm of forming sums of products coupled with a set of shift register modules is known to allow such a wide range of digital filter requirements to be met.
Modular Multiplier and Digital Filter for LSI Development

855

efficiently by varying the configuration of only three standard modules. And yet, the definition of the standard modules actually allows a maximum processing efficiency for the number of circuits required since there is a high level of parallelism both in the multiplier and the adder modules.

TABLE II—Maximum delay to form the 16-bit product of two 8-bit numbers using the modular carry advance multiplier

<table>
<thead>
<tr>
<th>Circuit Type</th>
<th>Sum Delay</th>
<th>Carry Delay</th>
<th>Multiplier Delay, ns</th>
<th>Multiplier Rate, MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN 5480 (II)</td>
<td>65</td>
<td>13</td>
<td>290</td>
<td>3.3</td>
</tr>
<tr>
<td>SUHL</td>
<td>42</td>
<td>10</td>
<td>156</td>
<td>6.4</td>
</tr>
<tr>
<td>(Sylvania)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MECL II</td>
<td>8</td>
<td>8</td>
<td>95</td>
<td>10.5</td>
</tr>
<tr>
<td>(Motorola)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MECL III</td>
<td>4</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Motorola)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SUHL</td>
<td></td>
<td></td>
<td>~50</td>
<td>~20</td>
</tr>
<tr>
<td>(with speed-up)</td>
<td></td>
<td></td>
<td>(Using Look-ahead and piping)</td>
<td>(Using Look-ahead and piping)</td>
</tr>
<tr>
<td>MECL II</td>
<td></td>
<td></td>
<td>~40</td>
<td>~25</td>
</tr>
<tr>
<td>(with speed-up)</td>
<td></td>
<td></td>
<td>(Using Look-ahead and piping)</td>
<td>(Using Look-ahead and piping)</td>
</tr>
<tr>
<td>MECL III</td>
<td></td>
<td></td>
<td>~30</td>
<td>~33</td>
</tr>
<tr>
<td>(with speed-up)</td>
<td></td>
<td></td>
<td>(Using Look-ahead and piping)</td>
<td>(Using Look-ahead and piping)</td>
</tr>
</tbody>
</table>

Comparison of the modular filter with a current filter processor

Table III presents a comparison of a current digital radar signal processing system with two LSI versions using the Modular Filter. Version I of the Modular Filter system uses 3/4-inch square flat-packs to package chips similar to those of Figure 12 and having typically 200 gates of logic. Version 2 is a full-wafer 1600 gate complexity LSI implementation requiring only three 2-inch square modules. Even Version I of the Modular Filter decreases the inter-package connections from 10,000 to 424 while reducing the number of packages from 1000 to 24 and the volume from 170 cubic inches to only 9. With this, ninefold gain in processing capabilities is obtained by the combined ability to process over twice as many range bins and to do 16 (rather than 4) unique filter phase shifts. Version 2 provides the potential lower cost and increased reliability of a full-wafer LSI system while obtaining further advantages in speed, volume, and interconnect. The modular partitioning techniques which efficiently define the standard filter modules permit these extreme advantages in physical characteristics, increased processing capability, and standardization, to be realized from the single-chip and full-wafer LSI technologies.

TABLE III—Comparison of a current processor and two versions of the modular filter

<table>
<thead>
<tr>
<th></th>
<th>Range</th>
<th>R/IO Cap</th>
<th>Multiplications Rate</th>
<th>Flat Packs</th>
<th>Volume With Mounting</th>
<th>Filter Characteristic</th>
<th>Connectors</th>
<th>Memory Delay</th>
<th>Lower with Reel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current digital filter processor</td>
<td>384</td>
<td>2 MHz</td>
<td></td>
<td></td>
<td>Brass-10,000</td>
<td>16 variable filter phase shifts</td>
<td>15, 385</td>
<td>Re</td>
<td></td>
</tr>
<tr>
<td>Version 1 of Modular Filter (Wafer LSI)</td>
<td>1104</td>
<td>16 MHz</td>
<td></td>
<td></td>
<td>1,080 x 24,000</td>
<td>16 variable filter phase shifts</td>
<td>125</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Version 2 of Modular Filter (Wafer LSI)</td>
<td>1100-1104</td>
<td>26-60 MHz</td>
<td>16-Rack modules</td>
<td></td>
<td>1,080 x 24,000</td>
<td>16 variable filter phase shifts</td>
<td>125</td>
<td>Yes</td>
<td></td>
</tr>
</tbody>
</table>

ACKNOWLEDGMENTS

The author sincerely wishes to thank Dr. Ira Terris and Messrs. R. F. Stewart, J. M. Block, C. F. Edge, and J. S. Steiner, all of Hughes Aircraft Company, for their helpful counsel and encouragement.