

# Bit access problems in 2-1/2D 2-wire memories

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## INTRODUCTION

The obvious cost advantage of a 2-wire 2-1/2D core mat over a 3-wire mat has, in the past, been offset by the increased complexity of the access and detection circuitry required for a 2-wire array. This paper will concentrate on 2-wire bit accessing schemes and describe one which appears to be cheaper and less noisy than the conventional bit access which uses a complete matrix per bit. It will then discuss the read-out noise problems. To predict the amplitude of noise a multistate core model similar to J. Reese Brown's<sup>1</sup> will be developed. The paper will then show how the individual core characteristics can be extrapolated to predict overall optimum memory performance.

### *Extrapolation of 2-1/2 D memories from 2 D memories*

The line drawing of a 32,768 word, 24 bits per word, 2-wire memory (Figure 1A) and the extension into two types of 2-1/2D (Figure 1B and Figure 1C) illustrates the derivation of both the typical 2-1/2D configuration<sup>2</sup> and the 2-1/2D configuration proposed in this paper.<sup>3</sup> In the 2-wire scheme, there are as many independent address lines as addresses and as many bit lines as bits per word. The example shown illustrates 32,768 address or word lines and 24 bit lines. Current on a selected address wire fully switches all cores whose signals are readout on the independent bit wires. Coincident currents on the selected address line and the independent bit lines are used to write back independent bit information into the selected word.

The first type of 2-1/2D memory which we call an independent bit matrix organization, segments each of the bit lines (typically 16 segments as shown in Figure 1B); independent selector circuits, one for each bit, are used to simultaneously select a segment for each bit. Since the bit lines have been segmented, the number of word lines can be reduced by a factor equal to the number of segments. The memory is read by

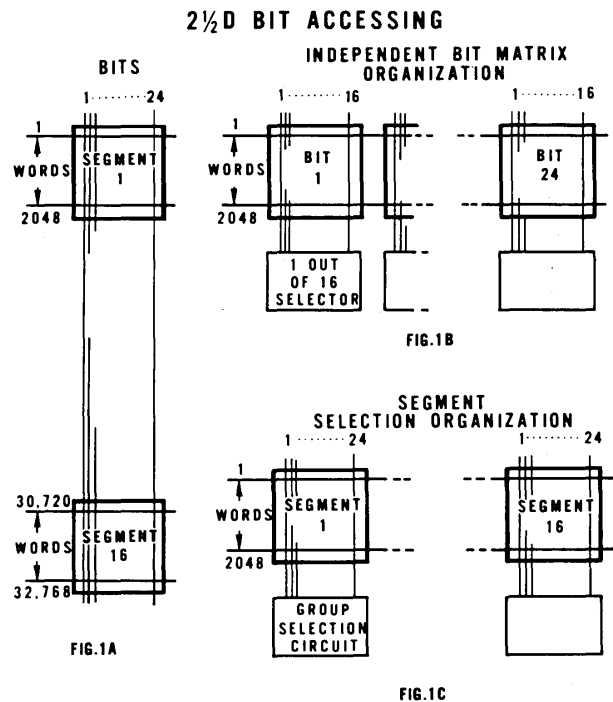


Figure 1—(a) Word organized, 32,768 word by 24-bit memory. (b) Conventional 2-1/2D realization of (a). (c) Segment organized 2-1/2D realization of (a)

sending a word current into the selected word line and simultaneously sending a bit current into the chosen segment of each bit. This achieves a coincident current selection of a core for each bit line. The bit segment selector circuits, although simple in function, are expensive and needlessly repetitious because there is a simultaneous decoding in each of the 24 bits; each selector making the same logical selection. For the memory on Figure 1B, the one out of 16 selector circuit requires at least 8 bidirectional or 16 unidirectional switches per selector and since there is a selector per bit, this scheme will require 192 bidirectional or 384 unidirectional switches.

A second form of 2-1/2D is a simple rearrangement of the segments as shown in Figure 1C. In this case, the adjacent segments of 24 bits are grouped rather than the 16 segments of each bit. The two-dimensional memory section called segment 1 in Figure 1A maps into the segment 1 section of the 2-1/2D memory in Figure 1C; the higher numbered segments map correspondingly. A single group selector circuit is activated and current is simultaneously sent to the 24 lines of the segment associated with that selection circuit. Word current is then sent to a selected word line. The simultaneous word current and bit segment currents select 24 cores in a word for readout. The group selection circuit is obviously a higher power circuit since it must deliver current to 24 lines but it has a much reduced logic decoding. A single one out of 16 selection must be made to pick the proper group selection circuit. This scheme, as will be shown later, can be realized with a total of 8 switches rather than the 192 or 384 in the alternative 2-1/2D memory, without materially affecting other component counts.

*Independent bit matrix*

A block diagram of the independent bit matrix organization is shown in Figure 2A. There is a word access selector shown at the left. The bit selection circuitry is made up of 24 independent matrices, one of which is schematically depicted in Figure 2B. The load at each matrix crosspoint contains two memory lines connected by a readout transformer, which also balances the bit current. The bit circuitry contains a total of 384 readout transformers, one for each pair of memory lines, 96 bidirectional switches, 192 unidirectional switches, and 768 bit access diodes. In addition, there must be some means of funneling the secondaries of the 16 readout transformers per bit into a readout detector. This could be done by using a low level selection switch per transformer for a total of 384 switches. At the expense of some loss in signal, one can connect several transformer secondaries in series as shown in Figure 2C, and thereby reduce the number of low level selectors required. In practice, it would be undesirable to connect more than four secondaries in series since the signal must then pass through the equivalent of 8192 cores. Therefore, at least 96 low level switches are needed.

*Segment oriented bit access*

The segment selection organization depicted in Figure 1C can be implemented by the configuration shown in Figure 3. The typical bit matrix of Figure 2B is replaced by an assembly of 16 diode bridge rails, one of which is activated to select a pair of memory lines

2½ D MEMORY WITH INDEPENDENT BIT MATRICES

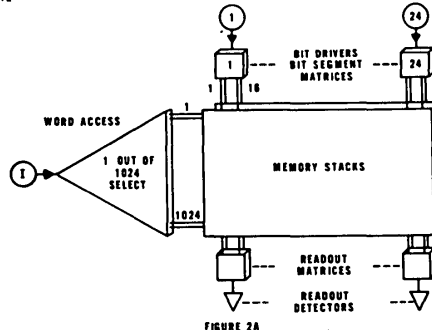
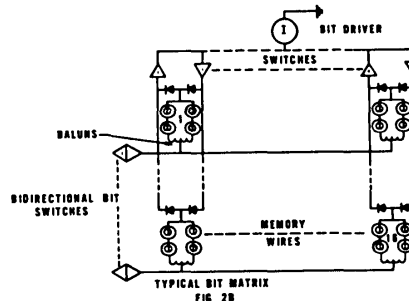
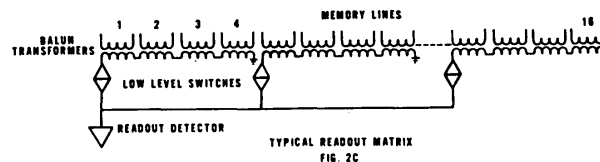


FIGURE 2A



TYPICAL BIT MATRIX FIG. 2B



TYPICAL READOUT MATRIX FIG. 2C

Figure 2—(a) Conventional 2-1/2D memory. (b) Typical bit matrix. (c) Typical readout matrix

for each bit. All of the diodes except for those associated with a selected rail are back biased by the +v and -v potentials shown on the left of Figure 3. This automatically isolates unselected bit lines so that the bit current driver will not send current through these segments and signals generated on the segments will be isolated from the readout transformer at the top.

The selected rail is activated by driving current through the primary (shown in Figure 6) of the transformer associated with the selected rail. This forward biases all diodes on that rail and provides a phantom ground to the lower ends of the pair of memory wires in each bit associated with the selected rail. This provides a current path for the bit driver and a signal path for readout to the transformer at the top.

This technique eliminates the need for low level selectors and requires only 24 readout transformers. For the short bit line segments being considered here, the transmission time of a bit line is short compared to the switching time of a core. Hence the effect of signal reflections due to the 15 open-circuited lines paralleling the selected line is slight. The capacitive

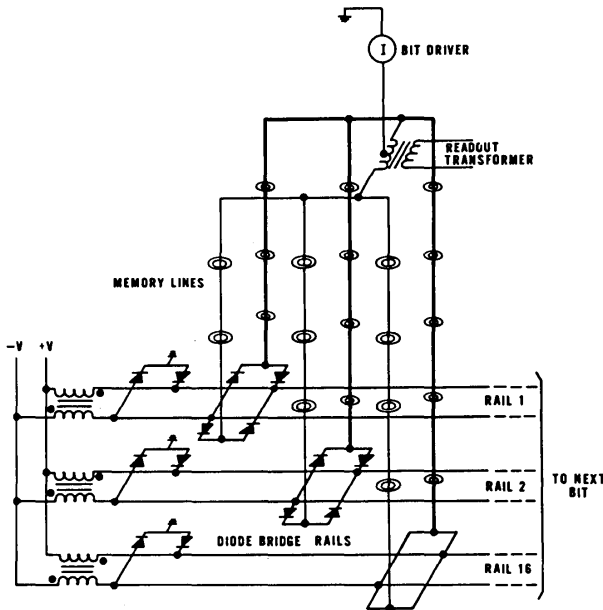


Figure 3—Group selection circuit with inherent readout selection

loading of these 15 lines on the selected line will tend to degrade the current rise time, but this can be minimized by sectioning the access into a multi-dimensional configuration which will be described later.

*Alternative organization*

There is an alternative organization which utilizes half the number of diodes, but increases the number of readout transformers. This scheme shown in Figure 4 is almost identical to the scheme shown in Figure 3; it contains 16 pairs of rails, but instead of having front and back lines independently connected to their own diode bridges, it couples the front and back segments by means of a balun-readout transformer. The center of the readout transformer is connected to the rails through a bridge diode configuration. The selected rail causes the bit current to flow to the selected front and back bit line while all other segments block current. The readout signals are coupled to the individual bit segment transformers. However, to obtain readout isolation, it is necessary, with this arrangement, to switch the secondaries of the 16 readout transformers by means of low level selectors to a common readout detector circuit.

*Multi-dimensional access*

The capacitive limitations imposed by paralleling many memory lines can be reduced by using the technique illustrated in Figure 5. The 16 pairs of lines of a given bit are divided into two groups, each of which is connected to a separate readout-balun transformer. The desired pair of bit lines is selected by simultaneously activating one of eight rails at the bottom and either Rail A or Rail B at the top. This method effectively halves the parasitic capacitance seen by the bit driver.

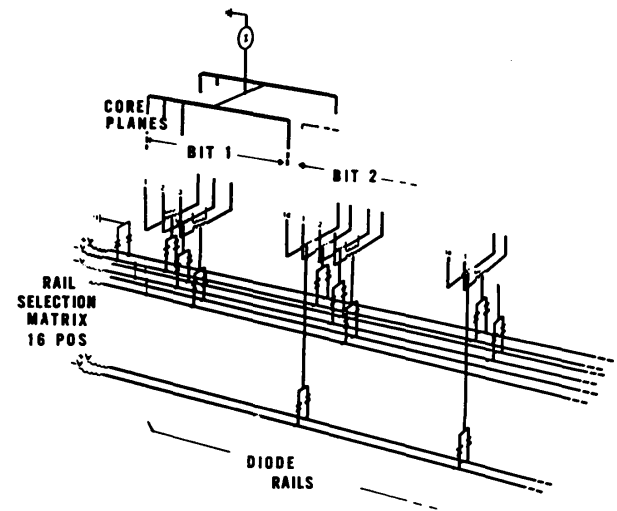


Figure 4—Group selection circuit without inherent readout selection

*Rail selection matrix*

The rail selection matrix shown in Figure 6 is an electronic 24 pole 16 position switch. At the right of the figure is shown a typical rail, normally back-biased. The rail is activated by current flowing out of the secondary windings of the transformer through the diodes with the grounded bridge node; this forward-biases all diodes of the multiarm bridges on the rail. Thus, each node is virtually grounded through the forward-biased diodes during the entire memory cycle regardless of bit current polarity on the bit segment wires. By alternating the direction of current on adjacent bits (shown by sending bit 1 current up and bit current 2 down during read time in Figure 6), the current handled by the transformer is halved. In effect, the transformer and grounded diodes merely switch the current from a bit to its neighbor.

The transformer primaries are themselves in a 16 crosspoint matrix containing 8 unidirectional 1 ampere

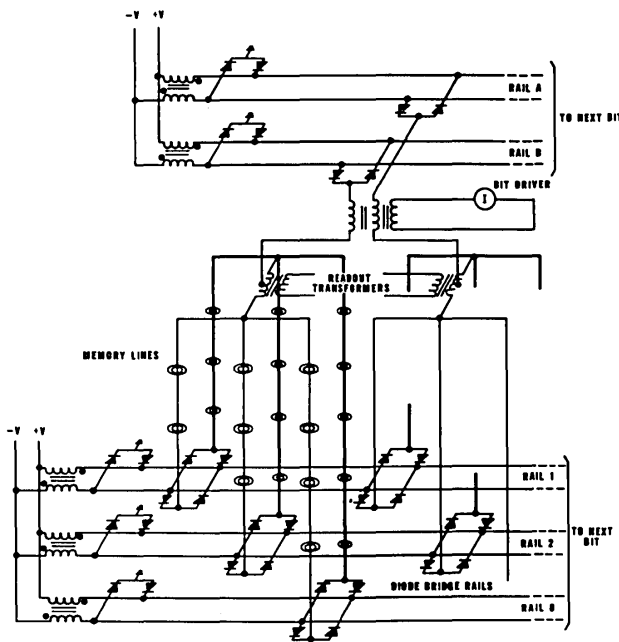


Figure 5 – Multi-dimensional group selection

switches. By selecting one of the four switches at the top and one of the four switches at the bottom, current is sent to one of the 16 crosspoints which, in turn, couples through the transformers to forward-bias a rail. In this drawing, we illustrate 6 transformers per crosspoint. This is done to limit the transformer current and rail current; by subdividing the rails, and cascading transformer primaries, currents in the order of only 1 ampere can drive an entire 24 bit word. In summary, the organization shown in Figure 6 has a number of distinct features. These are:

1. Bit segments are virtually grounded when selected so that no voltage drop is required by the access switch. This lowers the voltage to the bit current drivers and improves current control capability.
2. The selected bridge nodes have very low dynamic impedances because the current paths pass from one bit to its neighbor without having to transfer through long wire lengths with attendant parasitic inductances and capacitances. During the memory read time there will be an insignificant change of current out of the transformer secondaries and negligible net current into the ground of the reference diodes. Dynamically the current will flow down bit 2, through the bridge diodes and back up the bridge diodes into bit 1. The entire matrix, with the exception of the diode

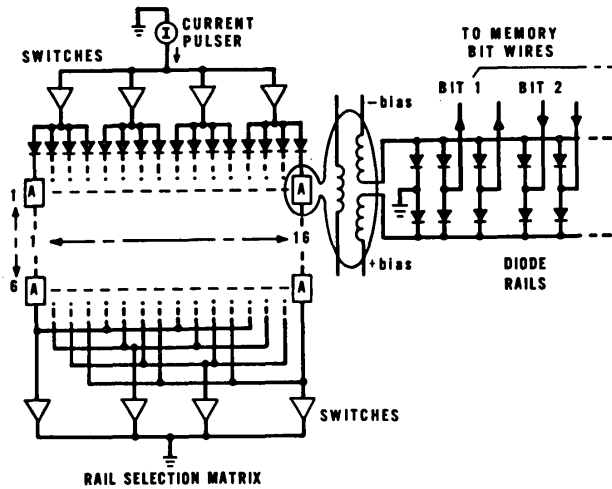


Figure 6 – 24-pole, 16 position bridge drive matrix

rails, can be remotely located from the core module without affecting current wave-shapes in the module.

3. Only 8 switches are required in the primary matrix to simultaneously select 24 pairs of segments out of 384.

A summary of component counts for the various access schemes considered is given in Table I.

Table I – Bit access and detection circuit counts  
32,768 Words      24 Bits/Word

	Segment Oriented Access			
	Conventional Access	Without Inherent Readout Selection	With Inherent Readout Selection	Multi-Dimensional
Access Switches	384	8	8	8
Access Diodes	768	960	1728	1752
Access Transformers	0	96	96	60
Readout Transformers	384	384	24	48
Low Level Selectors	96	96	0	0

*Influence of the core characteristics upon memory performance*

For a 2-1/2D 2-wire configuration the requirements of the core differ from the standard three dimen-

sional coincident current core. It is obvious that the memory output signal is heavily influenced by the noise generated by bit current shuttling the many cores of the bit segment wire. The readout transformer must measure a small core switching signal in the face of thousands of cores shuttled by half currents. This is an order of magnitude larger than the typical three dimensional memory, where the readout must be sensed in the face of only a few hundred cores shuttled by X and Y half currents.

To analyze the bit current noise, we make use of the 6 state hysteresis loop characteristic of the core shown in Figure 7. As will be seen later, it is desirable to operate the 2-1/2D memory with offset currents; i.e., bit current less than word current. For this case, a number of additional intermediate states exist. However, the worst case disturb condition is generated by the larger amplitude word current and we can neglect the less noisy intermediate states. The states are defined as follows:

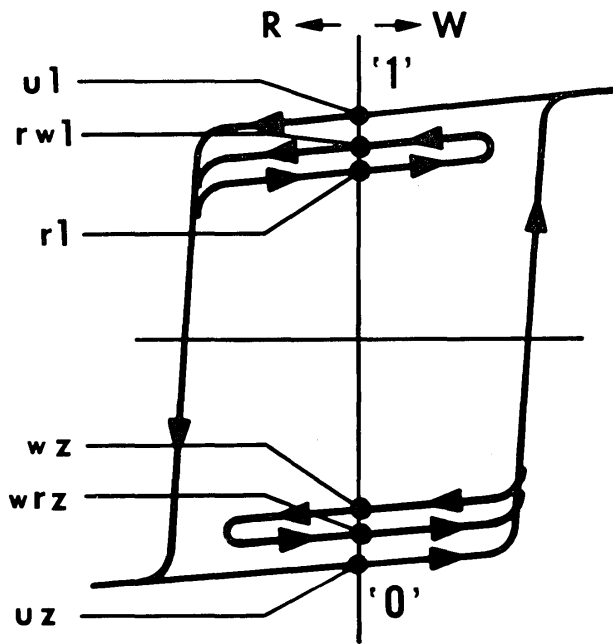


Figure 7—6 state hysteresis loop model

1. *u1* is the state arrived at when the core is switched by a full write current.
2. *rl* is the state arrived at when a core in *u1* is excited by a half read current. There is another state somewhat lower than *rl* called *dl* which will occur when the core is continuously excited by half read currents, however, the core outputs are almost identical in states *rl* and *dl*.
3. The state *rwl* occurs when a core in *rl* or *dl* is excited by a half write current.

4. Subsequent excitations of half read and half write currents shuttle the core between *rl* and *rwl*.
5. The state *uz* occurs when a core is fully switched by a read current.
6. The state *wz* occurs when the core in the *uz* state is excited by a half write current. Similarly, there is an upper state *dz* which is achieved when the core is repeatedly excited by a half write current. However, the difference between *wz* and *dz* is small as far as the core responses are concerned.
7. The state *wrz* is achieved when a core in the *wz* or *dz* state is excited by a half read current.
8. Subsequent excitations of a half read and half write current shuttles the core between *wz* and *wrz*.

A core in the states *u1*, *rwl*, *wz*, and *dz* exhibit irreversible flux switching when excited by half read currents. Irreversible domain wall motion occurs even for very low half read currents. Thus, there will be an output from cores in these states even after the exciting current rise time has expired. Figure 8 illustrates the effect for half read bit currents. The core in state *u1* has the *uVhl* output, *rwVhl* is the output of the core in state *rwl*, and *wVhz* is the output of the core in state *wz*. All of these responses exhibit a recovery tail due to domain wall motion even after the rise time of the excitation current. Cores in the states *rl*, *dl*, *wrz*, and *uz* exhibit mostly reversible flux when excited by a half read current; the output is negligible after the current rise time. This is illustrated in Figure 8 by *rVhl* (*rl* state), *wrVhz* (*wrz* state), and *uVhz* (*uz* state).

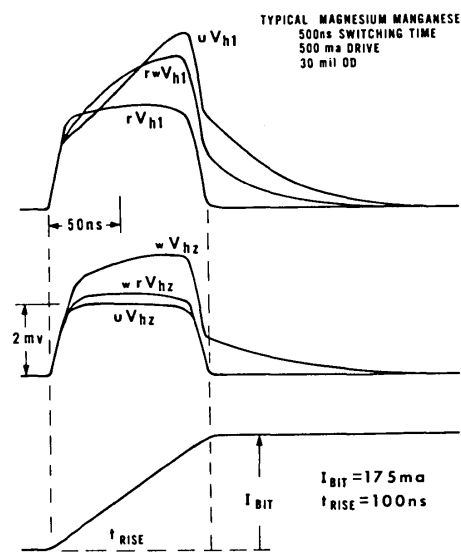


Figure 8—Core output waveshapes when excited by half-select bit current

For the 2-wire 2-1/2D memory shown, the bit half current will excite 1,024 cores in the front plane and 1,024 cores in the back plane whose output signals are sensed differentially in a readout transformer. If the cores in the front plane are in an irreversible flux state while the cores in the back plane are in a reversible flux state, a large recovery tail noise will occur. It will exist long after the bit rise time is over and will interfere with the signal output. In a 2-1/2D memory with a read regenerate or erase and write cycle, it is impossible to have any cores in the uz state and no more than one core can be in the ul state. Therefore, for practical purposes, the worst case will occur when all positive sensed cores are in the rwl state and negative sensed cores are in the rl or wrz state or vice versa.

#### *Word access wiring*

To improve memory performance, there is an obvious desire to minimize the number of cores in the front plane or the back plane that are in the irreversible flux state. Fortunately, there is a word access wiring technique that can reduce the number of irreversible flux state cores by a factor of two; the technique is illustrated in Figure 9. A typical bit loop with a readout transformer at the top, the bit drive current at the center of the readout transformer, and the bridge diode rails at the bottom are shown in Figure 9A. The bit drive current splits evenly between the front and back segments into the grounded nodes at the bridge diode. The transformer at the top not only senses the switching core output, but equalizes the current on the front and back plane because of its balun connection. However, the noise difference between the front and back cores due to bit current will show up as a differential signal across the readout transformer.

By wiring the word loops so that a word loop intersects two adjacent cores on the same bit segment and by separating front plane word loops from back word loops four distinct advantages result.

1. Either the upper or lower core of the pair excited by the word loop can be selected by the direction of word loop current.<sup>4</sup> Thus, the number of word loop accessing circuits are reduced by a factor of two.
2. The upper core will generate a noise that is opposite to the noise of the lower core when excited by word loop current and the readout transformer will see a cancelling signal from two adjacent cores; this will lower the noise due to the word loop current.
3. The most important advantage, however, is the fact that when the word loop current pulses, it

automatically drives one of the two cores into the reversible flux state. Thus, it is impossible to have more than half the cores on a bit segment excited by word current in an irreversible flux state. It can be shown that this cuts the bit line recovery tail noise in half.

4. The cores can be oriented in line rather than in a diamond pattern. This allows the cores to be on closer centers.

Figures 9B and 9C illustrate an additional advantage achieved with the word access wiring shown. In high speed memories it is also necessary to reduce the capacitance coupling between the word loop and the bit loop. Unfortunately, the word loop of Figure 9A couples to only one side of the bit loop. Thus, any voltage bounce on the word loop would capacitively couple into one side of the bit loop and would be sensed as a differential signal by the readout transformer. If we arrange the word loop access matrix as shown in Figure 9B so that half the word loops on any rail (vertical or horizontal) couple to the front segments of the bit loop and half to the back segments of the bit loop, then voltage bounces in the word access rails will generate equal capacitance coupling signals on the front and back segments of the bit loop. The readout transformer will not sense these signals; it will reject them as common mode noise voltages. Figure 9C illustrates physically how the word loops should be wired to realize common mode cancellations; the word loops interlace alternately between the front and back plane of the module.

#### *Memory signals*

Figure 10 illustrates the bit current excitation and the resulting output signal. The bit current is pulsed first to allow time for the recovery tail to expire. After recovery tail expiration the word current is turned on. A large inductive noise pulse will occur during the rise time of bit current. After rise time, there will be a bit line recovery due to irreversible flux switching. The recovery tail will ride upon a DC pedestal which is due to the difference in resistance and difference in diode voltage drops between the front and back plane. In this memory, therefore, the readout detector must sense the output signals with respect to the pedestal. A number of techniques can be employed such as DC restoration or delay line restoration;<sup>5</sup> the actual scheme utilized is a capacitance charging DC restorer. After restoration, the word current is pulsed to readout a "1" signal or a "0" signal from the selected core. The "0" signal will decrease after the rise time of word current so that during the peak of the "1" signal the major noise present will be the recovery tail due to bit current.

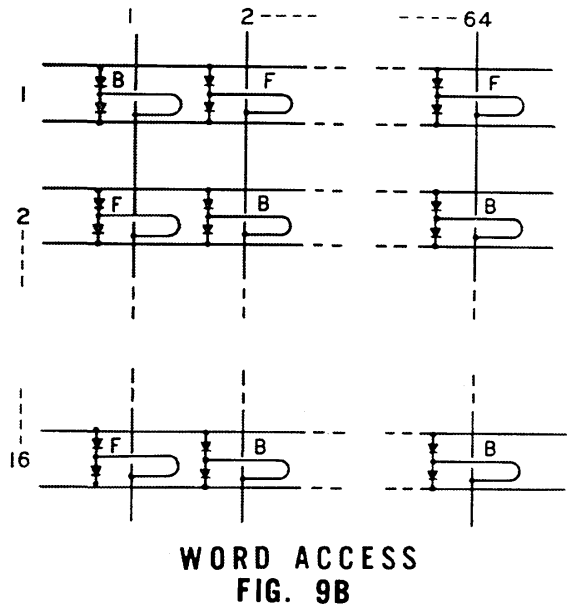
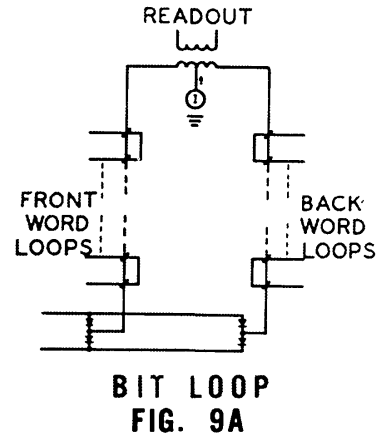
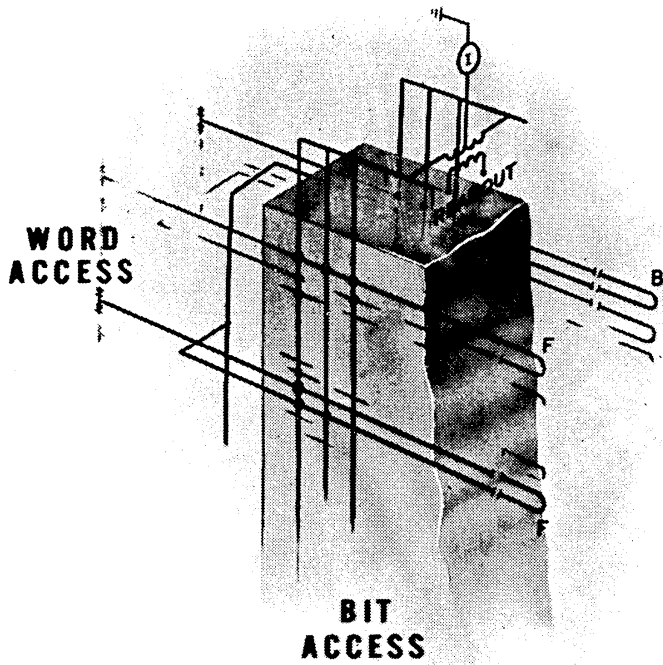


FIG. 9C

WORD ACCESS  
FIG. 9B

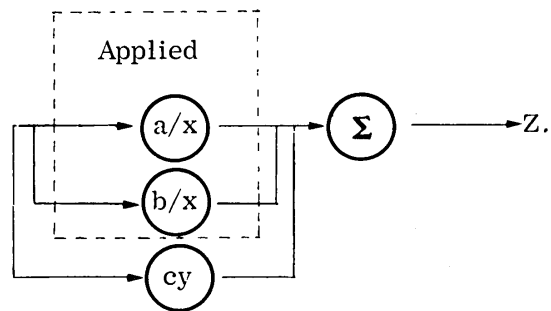


Figure 9—Word access wiring pattern for minimum magnetic and capacitive noise. (a) Bit loop. (b) Word access. (c) Pictorial representation

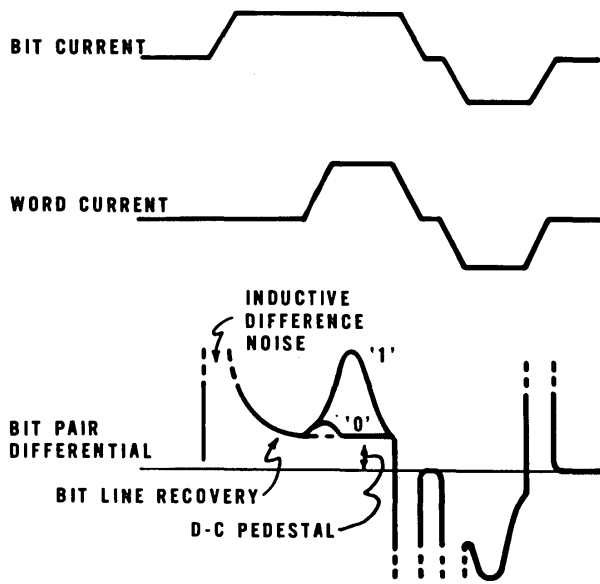


Figure 10—Memory current timing and readout waveform

Thus, it is evident that the signal to noise ratio is predominantly influenced by the bit line recovery tail and not by the "0" readout of the selected core.

To quantitatively prove this fact, we study the core characteristics shown in Figures 11, 12, and 13. The core characteristic in Figure 11A is the millivolt out-

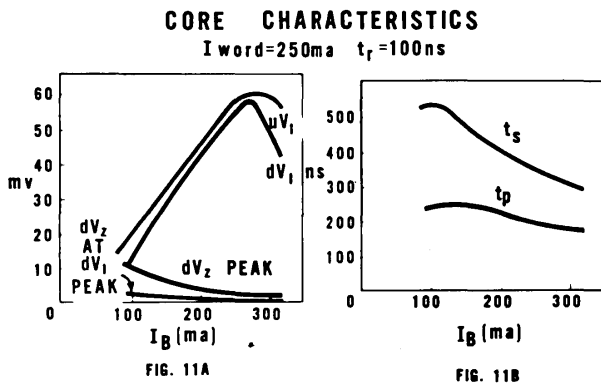


Figure 11—Core output characteristics for current timing as shown in Figure 10. (a) Readout amplitudes. (b) Time intervals.

put of a core switched by the coincidence of a bit current, whose amplitude is varied, and a fixed word current of 250 milliamperes with a 100 nanosecond rise time; the bit current is turned on first and the word current second as shown in Figure 10 to simulate the actual 2-1/2D operation. The output occurs during the word current, but we are plotting the output as a function of bit current amplitude. Two important conclusions can be drawn from this characteristic. First, the plot differs from the typical curves of most manu-

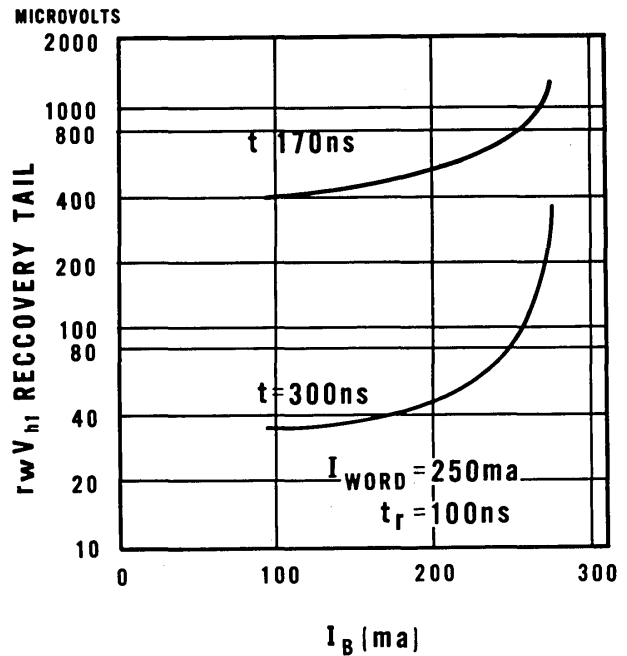


Figure 12—Amplitude of  $rwV_{hi}$  recovery tail as a function of  $I_B$  at fixed time  $t$  after start of  $I_B$

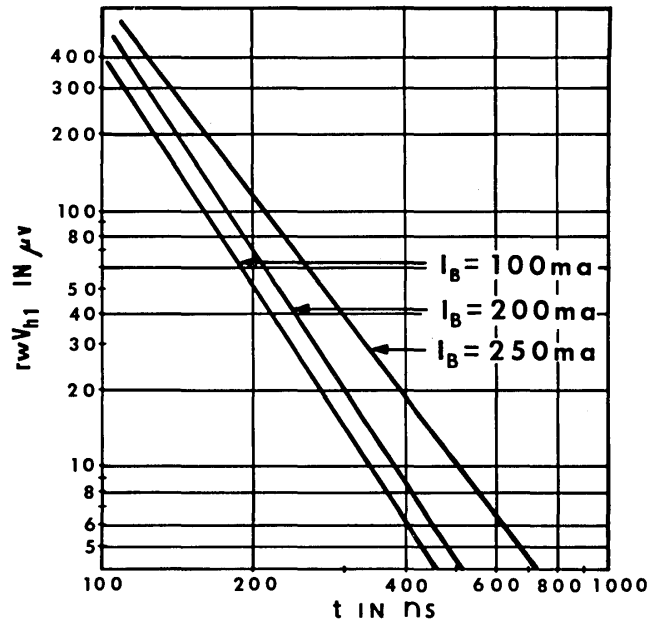


Figure 13—Amplitude of  $rwV_{hi}$  recovery tail as a function of time for various values of bit current

facturers because the manufacturers do not characterize the cores with a time staggered sequence of coincident currents. Secondly, the  $dV_z$  output at the peaking time of the  $dV_1$  is less than 1% of the "1's"



output even at bit currents of less than 150 milliamperes. Even though the dVl is maximum at 275 milliamperes, there is an obvious tendency to use low bit current to reduce the bit recovery tail; Figure 12 illustrates quantitatively how low bit currents reduce tail noise. A plot of  $\text{rwV}_{hl}$  versus bit current at 170 nanoseconds and 300 nanoseconds after start of bit current is a measure of the recovery tail for a core since the rise time of the bit current is 100 nanoseconds. For a bit current of over 250 milliamperes, the recovery tail becomes extraordinarily large and the memory noise due to irreversible flux increases rapidly. Even at low bit currents and at a recovery tail time of 300 nanoseconds, an output of 20 millivolts will occur from 500 cores, generating a noise close to 50% of a "1's" output. This proves that the recovery tail is by far the largest noise source and limits the performance of the 2-wire 2-1/2D memory. Figure 11 proves that we need high bit currents to get large dVl outputs up to a current of 275 milliamperes. Figure 12 proves that we need low bit currents to get low recovery tail; therefore, there must be an optimum to achieve best signal to noise ratio.

Figure 13 contains plots of the recovery tail as a function of time on a Log-Log scale for different bit current amplitudes. The straight lines indicate an interesting characteristic; the output voltage falls off approximately as the inverse of time squared ( $1/t^2$ ) for moderate bit currents. Another important conclusion exhibited by Figure 13 is that the recovery tail to 10% of the nominal core output (for bit lines of 1,024 cores) lasts for the order of 400 to 600 nanoseconds for a core with a switching time in the 400 to 600 nanosecond range. Thus, the recovery tail is as long as the switching time.

#### Signal to noise optimization

By combining the dVl output of Figure 11A, the switching time,  $t_s$ , (initial 10% to final 10% of dVl) and peaking time,  $t_p$ , (initial 10% to peak of dVl) characteristic of Figure 11B and the recovery tail voltage of Figure 13, it is possible to obtain a signal to noise plot as a function of bit current for the 2-1/2D memory. Figure 14 contains a plot of the signal (dVl) to noise (Recovery tail due to the bit current) for 1000 cores on a bit line as a function of bit current, with memory cycle time as constraint. The memory cycle time is defined as the read switching time plus the write switching time of the core plus the recovery tail time. This plot has been carried out for a typical 500 nanosecond, 500 milliamperes, 30 mil outer diameter core in a memory cycle time of 1.4 microseconds, 1.2 microseconds, and 1.0 microseconds. The result is that the best signal to noise ratio occurs at a bit

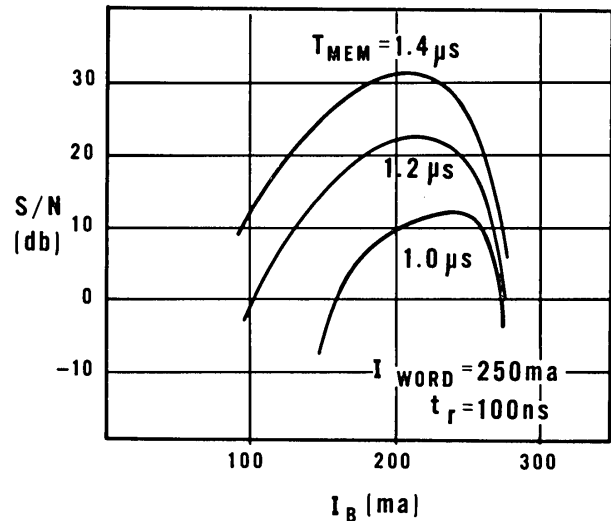


Figure 14—Ratio of  $dV_1$  to amplitude of  $\text{rwV}_{hl}$  tail at  $t = t_t$  such that  $T_{\text{mem}} = t_t + 2t_s$

current of 225 milliamperes; this is optimum at a bit current 25 milliamperes lower than the word current and 50 milliamperes lower than the peak "1's" output current. Similar data have been taken for many cores with almost the identical result. A converse plot, for a fixed signal to noise ratio, of memory cycle time versus bit current proves that minimum cycle time will occur at a bit current of 225 milliamperes. Thus, we can conclude that the best signal to noise performance and the minimum cycle time will occur at a bit current lower than the word current and under-driven to the extent of decreased "1's" output.

#### SUMMARY

In this paper, we have described a class of new access schemes that appear to be economic without degrading performance. An analysis of secondary and primary core characteristics has been carried out to assist in predicting optimum memory performance.

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