The B8500-microsecond thin-film memory

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INTRODUCTION

The computer in a B8500 modular data processing system may be equipped with as many as 16 memory modules, each of which has a capacity of 16,000 words of 52 bits each. The modules are self-contained with power supplies, logic circuits, and receiving and transmitting circuits which communicate with the computers.

The storage unit in a memory module is mounted in a single cabinet housing four memory frames with planar, ferromagnetic film storage elements. The films are interrogated in a linear select mode, in which a destructive "read" is followed by a "write" or a "restore" cycle. The half-microsecond memory cycle was chosen for reasons of economy and is not the upper frequency limit of a film memory.[1,2,3] In addition, four 52-bit words are always read during one memory cycle (fourfetch), because one thin-film word line embraces 208 bits.

The memory cell

The memory cell configuration was chosen which combined the film memory's characteristic high-speed switching behavior with a low-cost assembly technique. The packing density chosen yielded a reasonable sense signal and still allowed the employment of mass soldering techniques for the interconnection between the stack and electronic circuits.

The basic cell is assembled from paired substrates in which film spots are placed face-to-face, but separated by the word, digit, and sense conductors in a triplate arrangement. The separation between films is about 4 to 5 mils and tests have shown that magnetic coupling reduces the shape anisotropy by about 50 percent. The substrate pairs are enclosed with continuous ground sheets which provide the return conductors for the triplate arrangement of the word, digit, and sense line conductors. The triplate has the advantage that the fields generated by the return currents in the grounds cancel in the vicinity of the film cells, thereby reducing the effects of the disturbing field emanating from the neighboring word and digit lines. A disadvantage of the triplate is that because of this field cancellation effect, higher currents than those needed in the conventional strip line are required to generate a given field in the center conductor. However, improved memory cell performance and ease of assembly more than justify the increased current demand.

The magnetic thin-films are produced by vacuum desposition of Molypermalloy onto 3-mil thick glass substrates. The film spots are obtained by chemical etching. The spots are placed on 25-mil centers in the word direction and on 50-mil centers in the digit direction. A single glass substrate contains 3072 film rectangles.

Memory plane

Memory cross section

The memory cell previously described is mechanized as shown in Figure 1. The sense-digit lines and the word lines are fabricated from 1-mil-thick Kapton,* 1/2-ounce copper laminate. The sense-digit configuration and the word-line configuration are etched on separate pieces of laminate. The magnetic films on 3-mil-thick glass substrates are bonded to both sides of the sense-digit and word line laminates. Properly spaced copper ground planes complete the package.

Lattice construction

The basic element of the memory plane is the lattice assembly, as shown in Figure 2. Five sense-digit line tapes and four word line tapes are aligned and taped to a master with the ends of each tape precisely positioned. The group of tapes is then laminated into a lattice in a laminating press to assure uniformity of the cross section of the assembly. Next, 3-mil glass substrates are precisely positioned and laminated to

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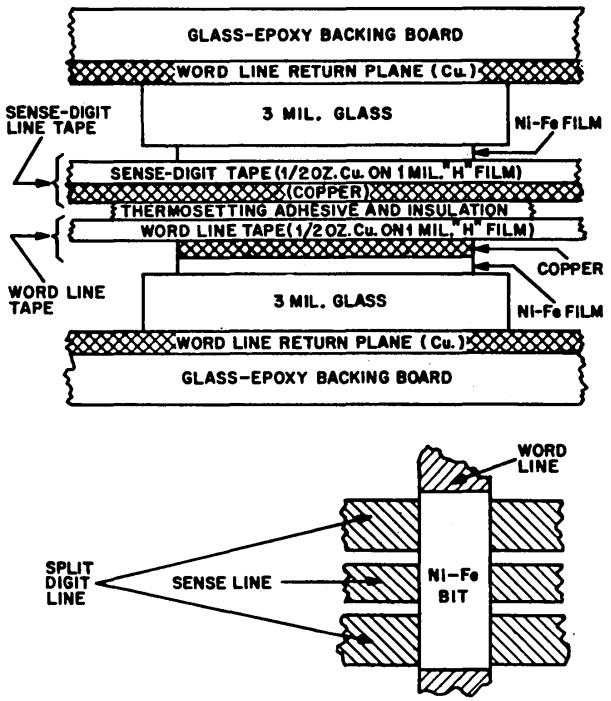

Figure 1 – Memory cell crossection

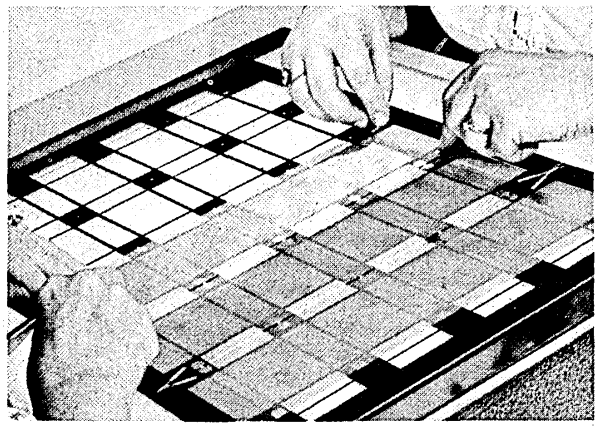

Figure 2 – Assembly of lattice

the lattice. Assembly criteria require that all portions of each intersection of a sense-digit group and a word line be covered by the corresponding magnetic bit. Special care is required to keep the magnetic film in intimate and consistent contact with the lattice. A gradated system of adhesives is used to maintain alignment during later laminating operations: (1) the copper-to-Kapton bond requires the highest temperatures, (2) the word-line-to-sense-digit tape adhesive system is intermediate, and (3) the substrate-to-lattice laminating system requires the lowest temperature.

The sense-digit cross section

Figure 3 illustrates the basic relationship of the sense and digit lines. This configuration was chosen to allow packaging of the digit drivers and sense amplifiers at opposite ends of the plane. The sense line crossover provides digit write noise cancellation. Assembly of four of the previously described lattices is illustrated in the exploded view. The triplate transmission line is mechanized with two outside ground planes (2-ounce copper laminated to glass-epoxy backing boards) and a solid copper inside ground plane. The inside and outside ground planes are electrically tied together at the periphery of the lattice.

The sense-crossover and digit feedthrough is made by using a three-level multilayer board assembly. The end-around functions are made by using an etched section of Kapton laminate wrapped around a glass-epoxy backing board. Sense-digit lines are terminated in printed-circuit boards which provide the connector interface to the digit drive and sense circuitry.

Word line cross-section

Figure 4 illustrates the basic relationship of the word lines in the memory plane. Triplate transmission line characteristics are maintained with the same inner and outer ground planes as previously shown in the sense-digit cross-section. The shorted end-word line is fabricated by soldering the bussed end of each word line tape to the inside ground. The word lines are placed on 25-mil centerline connectors but, because of the relative unreliability of 25-mil centerline connectors, the word lines are permanently tied to a printed circuit board which holds an 8×8 word-selection transistor matrix that permits a reliable connector interface on 0.100-mil centerlines.

Plane assembly techniques

Although the connector interface of the memory frame utilizes well-proven commercial connectors, the great number of solder connections necessary within the plane required a new connection technique that was both reliable and economical. The design of the memory plane internal connections was standardized using a process that can simultaneously solder many joints at a time. In each case, the end of a copper-Kapton laminated tape is reflow-soldered to a mating printed-circuit board. The etched copper-

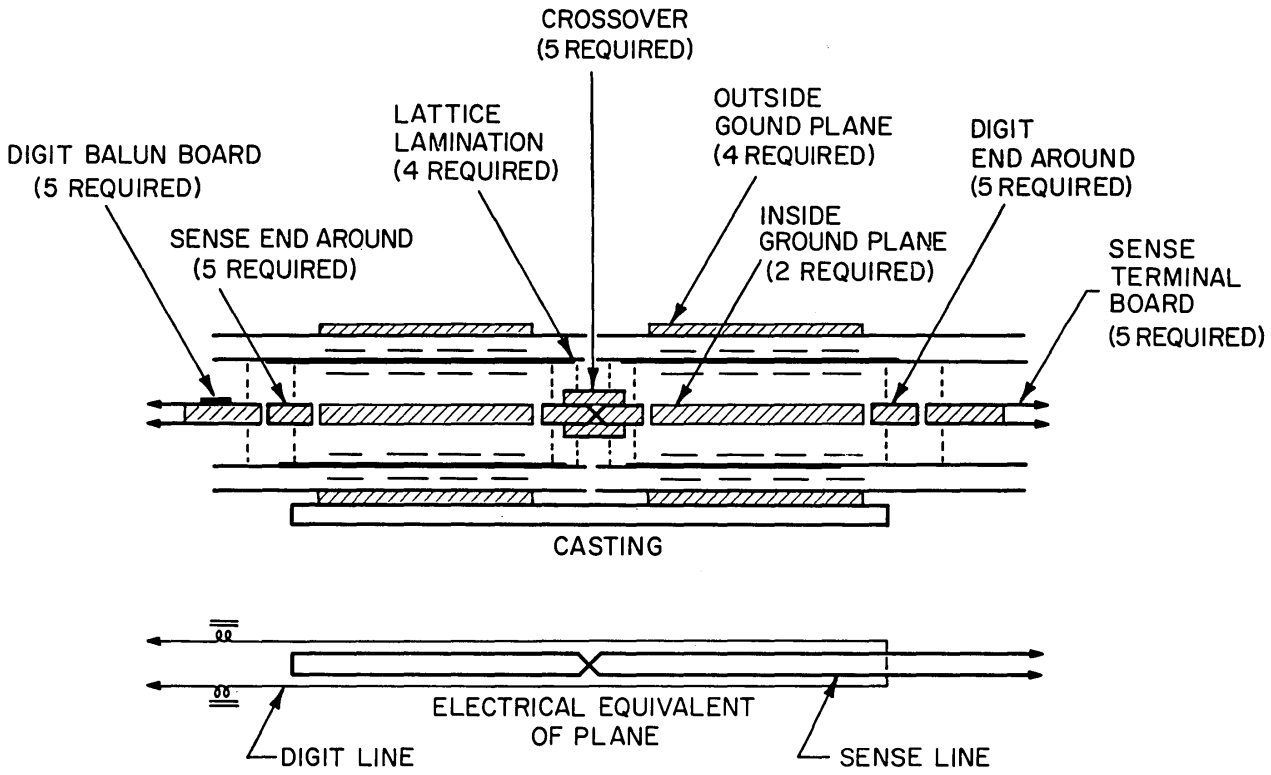

Figure 3 – Sense-digit lines crossection

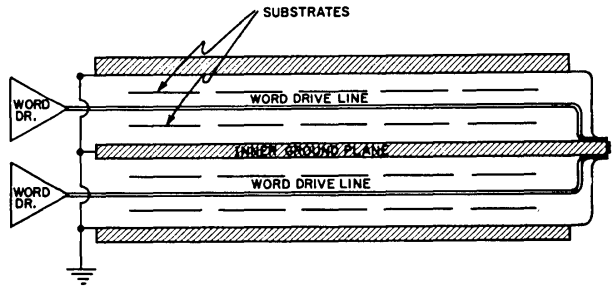

Figure 4 – Word line crossection

Kapton laminate and the printed-circuit board are then solder-plated to a closely controlled thickness and the plating is reflowed in hot palm oil.

A soldering machine was designed to apply a soldering blade to the Kapton side of the copper-Kapton laminate with the proper heat, timing, and distribution of pressure. The machine also provides the back-up and hold-down devices to ensure consistent, reliable reflow-solder joints. The heat is transferred through the Kapton to the plated conductors on the other side. These conductors have been previously aligned with plated conductors on the printed-circuit word. The temperature is adjusted for reflow of the solder at the interface of the conductors to be joined. To provide the maximum strength and reliability of the joint and a minimum of solder splashing between conductors, the following must be carefully controlled: temperature, pressure, cooling cycle, method of hold-down while cooling, and quality and thickness of solder plating. The plane can be indexed under the soldering head to previously set stops. The solder blade applications required for intraconnection of the plane can be made in less than one hour.

Memory circuits

The electrical interface and the logic functions are made using CTμL microcircuits. The current drivers and sense amplifiers are assembled in hybrid form utilizing Cermet silk-screened register-conductor patterns on alumina substrates. Semiconductors and capacitors are hand-soldered to the circuit chips.

Word drivers

Current to each word line is supplied by 1024 transistor switches which form a 32 × 32 matrix. The matrix is packaged on 16 multilayer cards containing 64 transistors each.

The 32 emitter drivers and the 32 base drivers energize the appropriate rows or columns in this matrix. All transistor switches are normally reverse-biased. Word current flows in a selected line when the emitter-output transistor saturates and supplies a negative current pulse to the appropriate emitter lines while the associated base driver removes the reverse bias from the selected transistor switch. A resistor between the emitter-driver output and the matrix controls the current amplitude. The word current has an amplitude of 600 ma ±10 percent and a rise and fall time of 15 to 20 ns with a duration of 150 ns.

The 32 emitter drivers and the 32 base drivers are packaged 8 to a card onto 4 printed circuits each. These 8 driver cards and the 16 word-matrix cards are interconnected through a multilayer backplane which forms part of the memory frame. (Refer to the subsequent paragraph and illustration describing the memory frame.)

Digit drivers

The digit drivers provide currents of either polarity and determine the future state of each memory cell after the word has been written into the stack. Digit current turn-on occurs while the word current flows and ends after the word current terminates.

The digit currents are supplied from two saturated-output transistors: one a PNP type for positive currents and one a NPN type for the negative currents.

The digit lines are shorted and resistors placed between the output transistor and the digit line control the current amplitude. The digit current has an amplitude of 150 ma ±10 percent, and a rise and fall time of 20 ns with a duration of 100 ns.

Sense amplifier

The nominal sense signal of ⅓ to ½ millivolt amplitude is amplified first by two differential stages followed by a threshold amplifier. The differential stages and the threshold amplifier are packaged on one hybrid chip each. The differential amplifier has over 45 db common rejection, eliminating the need for transformers at the amplifier input.

Memory frame

The memory frame shown in Figure 5 is made up of the memory plane and the memory circuits. Be-

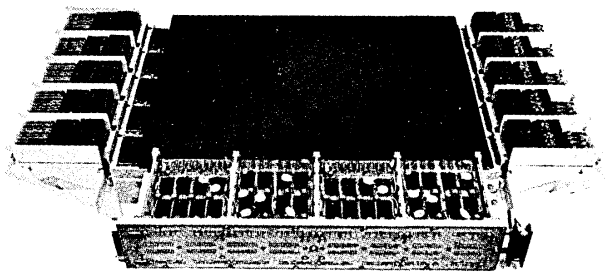

Figure 5 – Memory frame

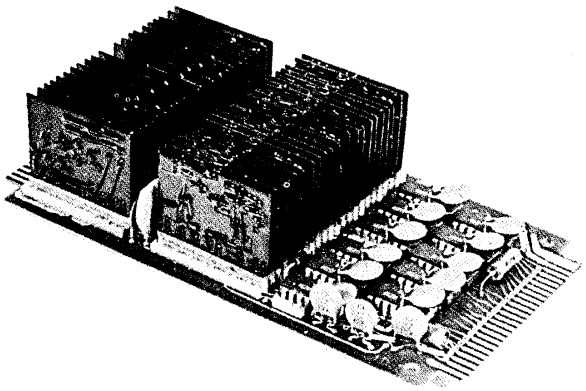

Figure 6 – Sense amplifier board

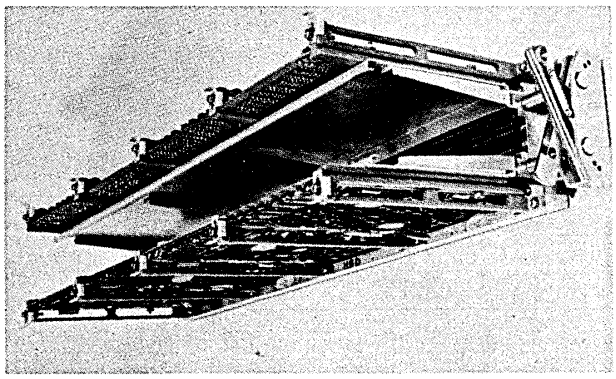

Figure 7 – Word address assembly

cause of the large ratio of power impressed on the memory to power-out of the memory and the proximity of conducting lines that allow crosstalk to occur. the memory electronics must be placed physically as close to the plane as possible. For this reason, the digit drivers, the sense amplifiers, and the word-address drivers are packaged integrally with the plane to form a memory frame. Each 1024-word X 208-bit frame has an interconnection level at the logic level (Fairchild CTμL).

The sense and digit circuit packaging is illustrated by the typical assembly shown in Figure 6. The sense amplifiers and digit drivers are each packaged on a hybrid circuit. The hybrid assemblies are plugged into receptacles on the mother board. The sense amplifiers and digit drivers are packaged on mother boards in groups of 22.

The 32 × 32 matrix which forms the 1024-address system for the memory is packaged as shown in Figure 7. The assembly interconnects the 8 × 8 matrix selection boards, which are a part of the plane, into a 32 × 32 matrix. The assembly also houses the 32 base and 32 emitter drivers which drive the word selection matrix. The interconnections for the selection matrix are fabricated using a 12-level multilayer printed-circuit board which maintains all interconnecting lines at 100 ohms characteristic impedance.

Memory organization

The 16,000 words of 52 bits each are stored in 4 thin-film memory planes as shown in the block diagram, Figure 8. Each plane has a capacity of 1024 words of 240 bits each, of which 208 bits are activated and the remaining 32 bits act as spares if needed. A film word line stores four computer words and every read cycle interrogates four words.

A 1024-word film plane contains word drivers, selection matrix, digit drivers, and sense amplifiers. The four planes share the address register, the information register, and the timing and controls circuits.

New words are written into the memory in 52-bit groups. If desired, all 208 bits can be loaded into the information register in four steps requiring 300 ns, after which all 208 bits are written into the selected address.

Memory timing

A memory cycle (Figure 9) begins with an initiate pulse and the gate pulse is sent to the selected base drivers 75 ns later. The emitter drivers receive their selected gate pulse at 100 ns. Emitter current to the matrix flows at 130 ns. Word current in the selected line interrogates the films at 140 ns. Sense signals appear at the differential amplifier output stages at 160 ns. The strobe pulse gates the sense signals into

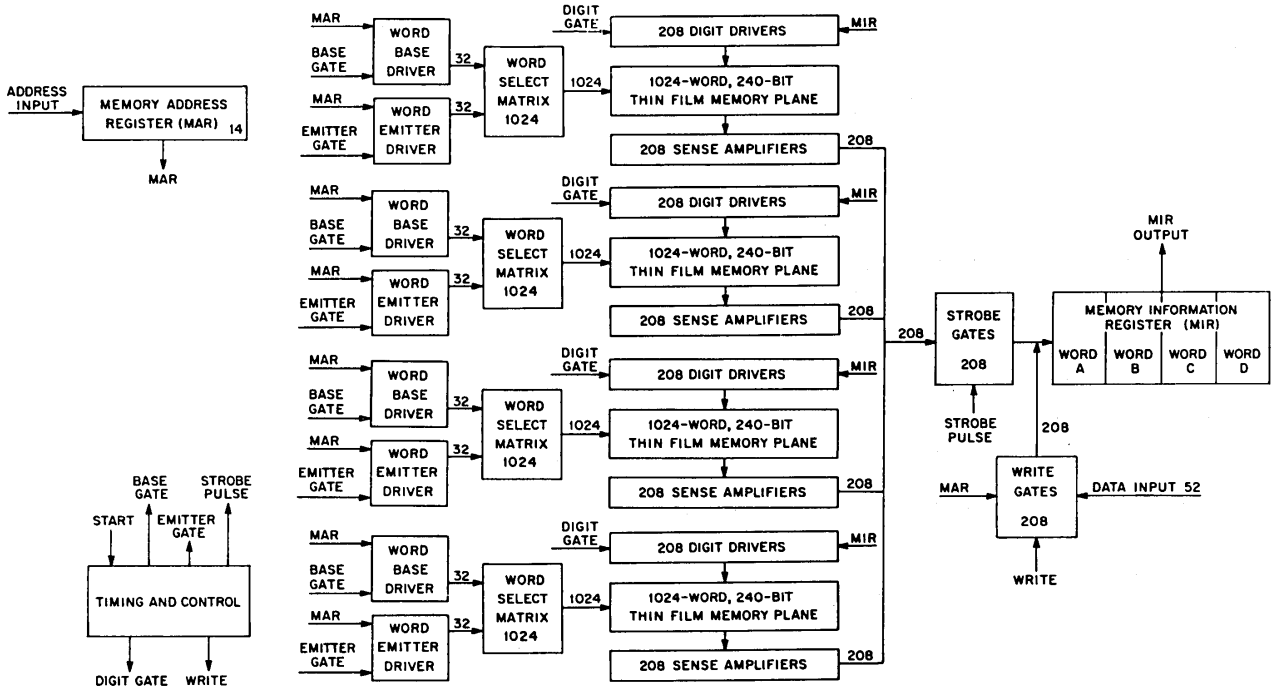

Figure 8 – Thin-film memory block diagram

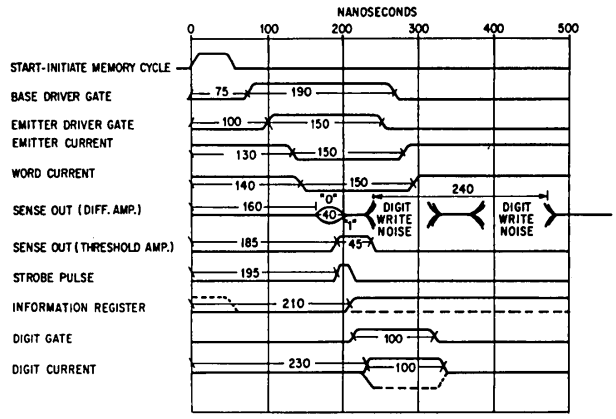

Figure 9—Thin-film memory timing diagram

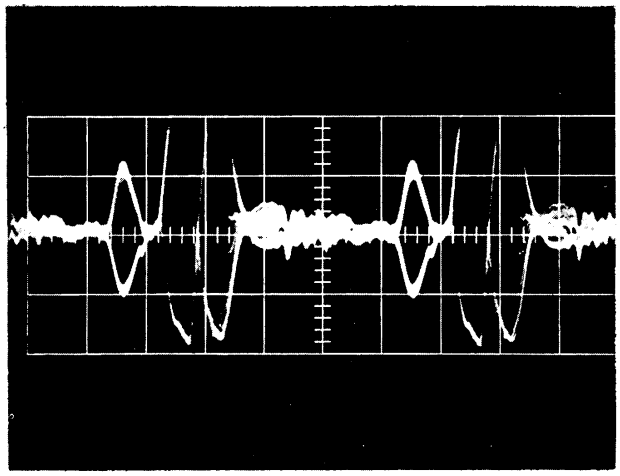

Figure 10—Sense signal waveform

the memory information register at 195 ns. The read data appears at the information register output before 210 ns. The restore or write cycle begins with the digit gate pulse at 215 ns. Digit current begins to flow in the plane at 230 ns and lasts for 100 ns. Word current turn-off occurs before digit current termination at 285 ns. Digit current turn-off at 330 ns completes the memory cycle. The additional time to make up 500 ns is needed to allow the sense amplifier to recover from the digit write noise. Typical sense readout signals from the memory stack are shown in Figure 10.

The memory stack

Each memory frame contains 1024 words, 208 bits long. Four of these frames are interconnected at the logic level. The associated circuits which these four frames share are packaged in a configuration similar to a memory frame. The interconnection is as shown in Figure 8. The frames slide into articulating connectors which are mounted on interconnecting controlled-characteristic-impedance multilayer printed-circuit boards. By opening an articulating connector at both top and bottom, any frame can be slid out for maintenance or replacement.

CONCLUSION

Fabrication, assembly, and operation of these half-microsecond memories has proven that large numbers of reliable film substrates are producible and that the completed memories can compete in both speed and price with the high-speed 2-1/2 D-type core memories. The future for planar films looks very bright; both larger and faster memories are in the design stage. These memories will combine the economic advantages of batch fabrication with the fast switching properties of thin-films.

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