A family of linear integrated circuits for data systems

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INTRODUCTION

The rapid expansion of automated digital data processing has created a need for low-cost analog data acquisition, display and control equipment. This implies low-cost D/A and A/D conversion equipment. This paper describes the resulting family of linear integrated circuits satisfying this need.

Conversion subsystems requirements

The principal parameters affecting the broad utilization of data converters are speed, accuracy and cost. Traditionally, higher word rates and accuracy are demanded of analog to digital converters than that of digital to analog. This is because: (1) multiple measurements are time multiplexed for encoding by a single A/D, whereas D/A commonly are used singularly; (2) A/A measurement range is employed wastefully for greater input flexibility, whereas analog output range tends to be standardized; (3) analog displays are limited in accuracy and speed by the resolving power and frequency response of the equipment as well as the resolution capability and flicker response of the eye; (4) high speed transient phenomena have to be measured in real time but are generally presented in post time; (5) A/D's generally operate bit-sequentially compared to D/A's operating bit-parallel.

A survey of data acquisition, display and control systems has shown an acceptable specification compromise between volume converter usage and mass production capability to be:

D/A Conversion

Rate	DC to 50K words/sec.
Resolution	8 to 10 Bits
Accuracy	±0.2% (full scale) ±0.1% (non-linearity)
Analog Range	0 to +5V or 0 to +10V
Output Current	20ma
Reference Voltage	Internal
Logic Compatibility	Bipolar (Micrologic families of CCSL, μL, RTμL, MWμL, DTμL, TTμL, and CTL).
Code Format	Binary or BCD
Temperature Range	O°C—70°C (Industrial) —55°C to +120°C (Aerospace)

A/D Conversion

Put-through rate	DC to 100K words/sec
Resolution	10 Bits
Accuracy	±0.05% (non linearity) ±0.001%/day (fullscale drift @ +25°C) ±0.001%/°C (fullscale drift with temp)
Analog Range	0 to 5V or 0 to +10V.
Analog Input Impedance	>1 megohm
Reference Voltage	Internal with external trim optional
Logic Compatibility	Bipolar (Micro logic families of CCSL, μL, RTμL, MWμL, D7μL, T7μL, and CTL)
Code Format	Binary or BCD
Temperature Range	0—70°C (Industrial) —55°C to +125°C (Aerospace)

Selection of a conversion technique

The goal of the subsystem design was to satisfy the stated specifications at a minimum cost to both the manufacturer and user. Therefore the design economics

must be considered first in the selection of a conversion scheme. The prerequisites for low cost for the manufacturer are:

1. Batch fabrication
2. High volume
   a. Minimum number of different chip types
   b. Each component independent functionally and individually saleable
3. High processing yield
4. Minimum amount of hand assembly work such as lead bonding.
5. Capable of simple or automated testing.

The prerequisites for low cost to the user are:

1. Easy to understand and use
2. Minimum number of external components and connections for assembly and test
3. Minimum number of device types to procure and stock
4. Compatible with existing hardware
5. Flexible in design so may be adaptable to many different applciations within the user's system(s) and product lines.

The factors thus stated imply a system which utilizes integrated circuits to the maximum extent permitted by the existing semiconductor technology. Monolithic construction provides the means for low cost production and a large number of functions per package, thus minimizing interconnections while enhancing system reliability.

The subsystem specifications of speed, temperature performance, and long-term stability could only be satisifed by bipolar transistor design for both the linear and digital portions of the circuit. Also, the logic levels and power supply voltages required for other than bipolar design would not be compatible with the majority of existing data equipment.

Preparatory to circuit design the known ADC and DAC configurations were studied.[1] Those techniques that would satisfy the subsystem performance specification and allow a major portion of the functions to be monolithically integrated were cataloged for component type and approximate count. A summary is tabulated in Figure 1.

The choice of a D/A technique was limited to either switched voltages/currents or switched resistors. Current switching was chosen because: (1) it is independent of switch off-set voltages; (2) it is fast and may be accomplished with a minimum of transient problems; (3) control circuit isolation is easily accomplished; (4) mutual isolation of current sources and output is easily accomplished.

The A/D techniques ranging from the ramp counter to cyclic, successive approximation, multi-comparator, ripple-through and parallel types were considered.[2,3] The choice was simplified by the following: the ramp-counter types are too slow; multi-comparator, ripple through and parallel types require excessive circuitry; and the cyclic types require accurate voltage switching in conjunction with large external capacitors. A D/A feedback successive approximation converter easily satisfied the performance specifications and could use the D/A as a feedback element. It offered these salient advantages:

Type of Converter / Required Components	D/A Techniques		A/D Techniques				
	R-2R Resistive Ladder	Weighted Voltages or Currents (Binary BCD Octal)	Cyclic (X2)	Cyclic (Charge Division)	D/A Feedback (R-2R)	D/A Feed-back (weighted) VOR1)	Cascade X2
Analog Switches	20	10	7	10	10	10	20
Precision Resistor	21	10	0	0	21	10	0
Precision Capacitors	0	0	0	3	0	0	0
" Gain Amps(fast)	0	0	2	1	0	0	10
" Gain Amps(slow)	1	1	1	1	1	1	1
" Ref Source	1	1	1	1	1	1	1
" Comparators	0	0	2	1	2	1	10
Large STORAGE Capacitors	0	0	2	3	0	0	0

Figure 1—Required component comparison for 10 bit converters

1. Generally well-known and understood and thus easy for the user to become familiar with, and use.
2. Versatile as the same building blocks may be employed for both A/D and D/A operation.
3. Coding flexibility—applicable to any D/A code.
4. Adaptable to all IC functional blocks for ultimate economy. The commonality of chip types for A/D and D/A means lower development and manufacturing costs.
5. The functional blocks are independently saleable products.

Because of the above considerations the design centered around a bipolar current summing D/A converter. The problem became one of defining the subsystem breakdown on a circuit building block basis, relative to IC technology capabilities.

DA converter configuration

Functional blocks needed for the DA subsystem, as shown in Figure 2 include:[4]

1. Transimpedance Amplifier
2. Logic buffer/current switching
3. Current sources
4. Voltage reference
5. Data register

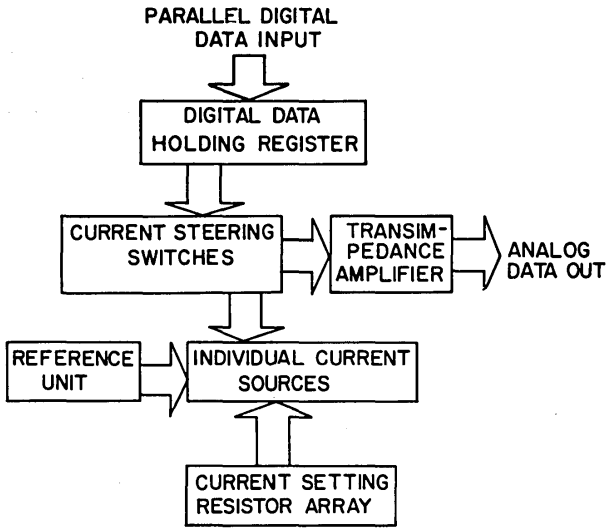

Figure 2—Current summing digital to analog converter functional blocks

Adequate integrated summing amplifiers are currently available in large quantities. Because these amplifiers find application in other areas their production volume is already high and their price, therefore, attractive. Further, such a choice allows the user to make the cost/performance compromises and tailor the converter to his specific system requirements.

A simplified version of the current switching circuit is shown in Figure 3A. It is apparent that current will flow through the diode whose anode is at the higher potential. By maintaining the output of the current switch at a fixed potential the current flow can be determined by applying various voltages to the "control" terminal. One disadvantage of this circuit is that the control potential must be capable of supplying all of the switched current. A significant improvement on this circuit is realized by driving the control from an emitter follower as shown in Figure 3B. The addition of a current source level shifts the control potential low enough in the "ON" condition to insure full current flow in the output. Summing any number of switched currents takes place by merely connecting the outputs of two or more current switches in parallel. However, care must be exercized to insure that the reverse diode leakages are small to minimize error current in the output. Quality silicon fabrication gives adequately low leakage over the temperature range for ten switches in parallel. Even though the switches are not gold doped, recovery is rapid enough for the required megabit operation since only one diode per switch is saturated.

To complete the explanation of the D/A converter

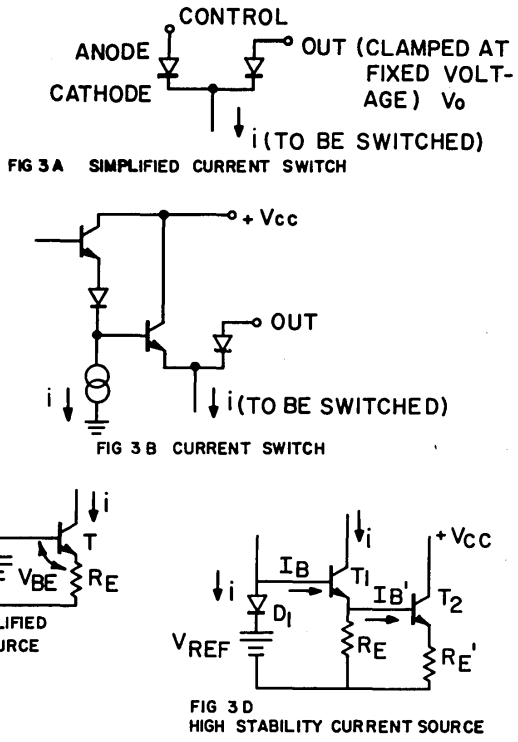

Figure 3

scheme, only the generation of accurate and stable currents remains. Typically in bipolar circuitry, current sources are made using the basic circuit shown in Figure 3C.

The collector current of such a circuit is given by $i_c = \alpha\frac{V-V_{BE}}{R_E}$. For most transistors, α approaches unity and V_{BE} is a logarithmic or weak function of collector current. As a result a reasonable current source is obtained. Because the output conductance of most transitors is low, the collector voltage of the current source has little effect on the collector current. For DA conversion where high accuracy and stability of the current value is required, steps must be taken to eliminate the collector current dependence of α, and thermal variations of V_{BE}. In Figure 3D a more complex current source is shown which remedies these variations.

The circuit is designed so that $I_B = I_B'$, therefore forcing the collector current equal to the current through R_B, the current determining resistor. This eliminates the dependence of the collector current I_c on the transistor current gain, α. Because T_1 and T_2 are on the same chip only a few mils apart, their characteristics are closely matched. In addition the use of high gain transistors minimizes $|I_B - I_B'|$.

Because a 10 bit converter requires 10 current

sources whose currents must be related in a binary manner, the V_{BE} dependence of I_C must be accounted for. Fortunately the collector current density is given by $J_c = J_{(sat)} \exp \frac{qV_{BE}}{kT}$ for many orders of current magnitude and over the military temperature range.[5] Thus, by knowing the design current value, a given V_{BE} may be determined and compensated if the emitter areas are held such that

$$\frac{I_c}{A} = \frac{I_{sat}}{A} \exp \frac{q V_{BE}}{k T}.$$

Much experience has been obtained in the matching of transistor parameters through the production of differential operational amplifiers. This experience indicates that the fabrication implications of such a requirement are not severe. Since D_1 has similar geometry to T_1 and its current matches T_1, the temperature dependence of V_{BE} may be compensated. Thus, by choosing appropriate values of R_E, stable current generators are available. The technique of combining this type of current source with current switching makes switching speed independent of mode capacitances in the current setting resistors, because the current continuously flows through the precision resistors.

None of the preceding considerations precludes the combination of the switches and the current sources on the same chip. Indeed, the use of high gain transistors improves the quality of the current sources, while the longer lifetime material required by these transistors decreases the leakage currents in the switches. However, a compromise must be made in the minority carrier lifetime of the material, for if it is too long, switching speed will degrade.

It is also apparent that the value of the current sources will depend on the value of the reference voltage. Because a zero temperature coefficient reference can also be fabricated using the high gain process, this too was included in the chip. Provision was made for the user to supply his own external reference for either (1) greater stability or, if required, (2) analog multiplication.

The digital register was not included on the current source chip for the following reasons.

1. Marginal speed without gold doping.
2. Incompatability with high gain used in the current sources.
3. Chip size would be inordinate for quantity production with present state of the art.
4. Avoidance of possible redundancy with respect to digital system registers.

With very few compromises it is possible to integrate the current sources, the current switches and the reference on the same chip at no loss of versatility for the user and considerable gain in ease of use. By leaving the precision resistors off the chip the user may use whatever codes he desires, thus enhancing flexibility.

With the inclusion of these three functions on the silicon chip, an area 60 by 160 mils was required. By using a proven process and designing with non-critical masking tolerances, the best possible yields were assured for this large circuit. In addition, the circuit utilizes only NPN transistors, ten of which require matching equivalent to integrated differential amplifier input transistors. The proven process consists of the standard 6 mask, monolithic epitaxial integration typical of currently available LIC's. Figure 4 shows the circuit.

In the final D/A configuration (Figure 5) the integrated blocks consist of the data register, the summing amplifier, the binary weighted current sources with the switches and reference, while the resistors are separate. The use of these functionally independent blocks allows the system designer to meet his conversion requirements at minimum cost.

The D/A performance curves for full scale drift and non-linearity versus temperature are shown in Figures 6 and 7.

A/D converter configuration

As mentioned earlier the DAC is utilized as a feedback element for a high speed successive approximation analog to digital converter (see Figure 8). The general comments made for the D/A converter apply also for the A/D converter. Operation of the A/D configuration in Figure 8 is as follows:

The logic programmer will successively try each data bit starting with the most significant (MSB). The programmer will monitor the comparator output to determine if the bit value is too large or too small. If not ($I_S R_S \leq V_X$), the comparator will cause the digital data register to hold the bit in. If the bit value pulls the summing bar negative ($I_S R_S > V_X$), the comparator will cause the logic to remove the bit. The programmer then will try the next bit in succession until $V_S \rightarrow 0$ and the digital equivalent of the analog signal (V_S) is stored in the register.

The summing current levels of the DAC, for 10-bit operation, are not directly compatible with the temperature-dependent offset current of most presently available IC comparators (e.g., μA710). A thermally stabilized differential pair μA726 may be used as an excellent buffer stage. For moderate temperatures, a simple differential pair is satisfactory. IC comparators of the μA710 class may be used directly for high speed, low accuracy operation (i.e., 6 to 7 bits) over a limited temperature range.

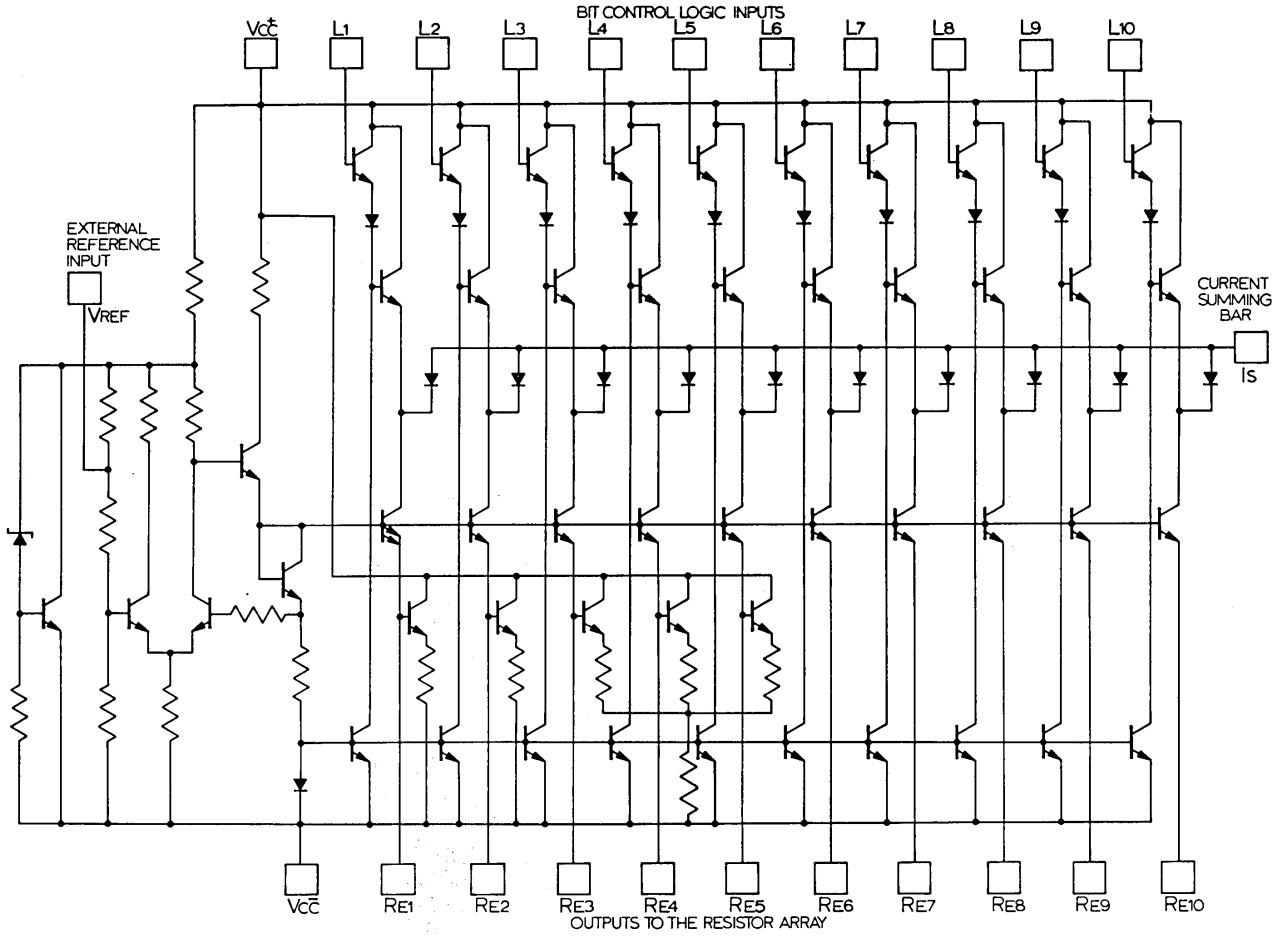

Figure 4—I.C. digital to analog converter

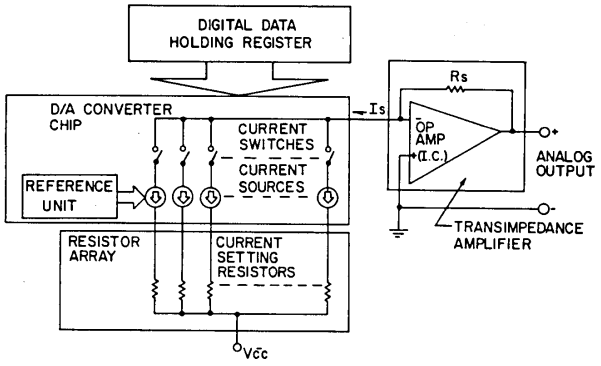

Figure 5—Current summing D/A converter I.C. blocks

Another solution is the use of a high slewing rate operational amplifier driving a comparator such as the μA710 in the place of the IC comparator. At present there is a high slewing rate (30V/μsec) operational

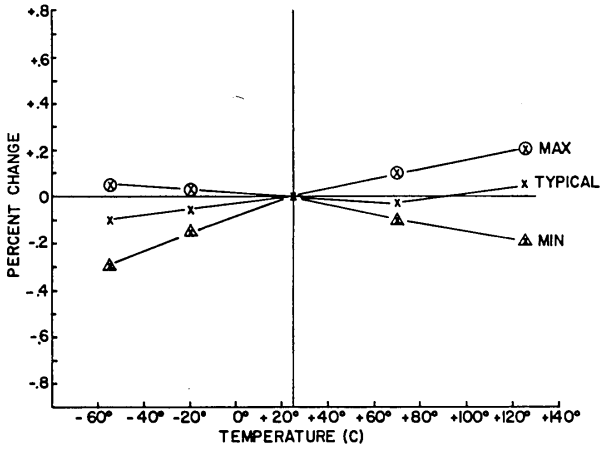

Figure 6—Percent change in full scale current vs temperature

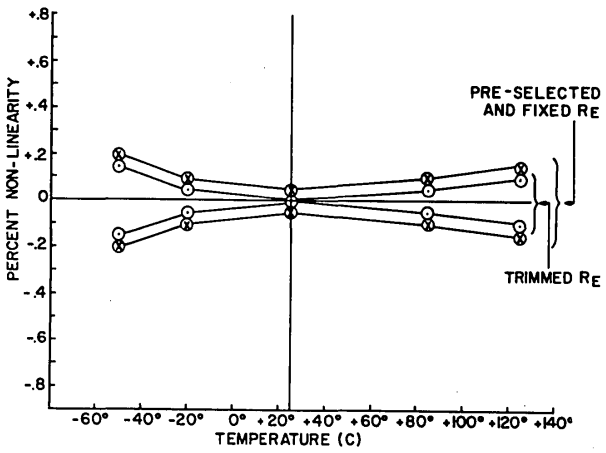

Figure 7—Percent non-linearity vs temperature

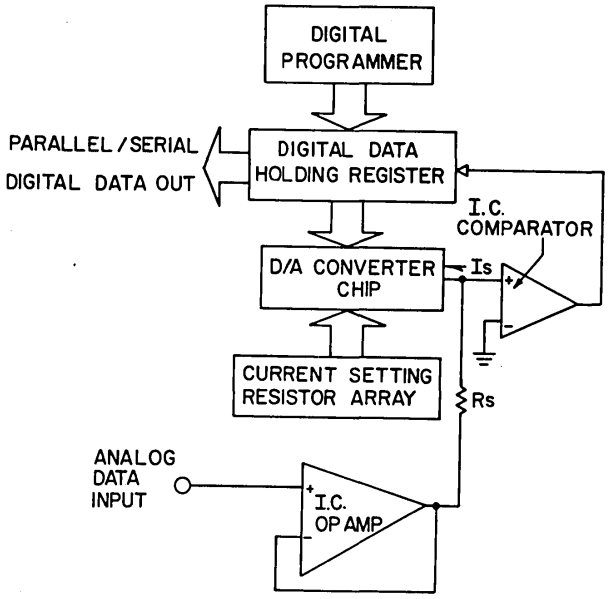

Figure 8—Successive approximation current summing A/D converter

amplifier in development capable of operation in this configuration.

Eventually a precision IC comparator (in development) will be available which is directly compatible with the D/A current sources and requires no buffering. Performance of the new comparator amplifier is summarized as follows:

V_{offset}	OmV (externally trimmed)
$V_{offset(T)}$	5μV/°C
I_{offset}	25nA
$I_{offset(T)}$	1.6nA/°C
$\tau_{switching}$	300 nsec.
V_{in} range	±5V
Common mode rejection	90dB
Power supply range	±6V to ±15V
Power supply rejection	100μV/v

Its outstanding input characteristics are made possible by a new IC process which provides substantially reduced offset current and current noise, in conjunction with higher transistor gain than present linear IC processes.

The new comparator will permit up to 13 bit resolution and similar accuracy. With nominal temperature stabilization 15 bits can be achieved.

Performance of the IC converters

A typical D/A converter is shown by Figure 9. The performance that may be expected is:

I.C. D/A Performance Parameters

Rate	DC to 50K words/sec.
Resolution	10 bits (Binary)
Accuracy	±0.2% (full scale) ±0.05% (non linearity)
Analog range	Variable 0 to +12 volts (Max)
Output current	20ma.
Reference voltage	Internal with optional external trim
Logic control levels	"1" less than +0.5VDC "0" greater than +2.5VDC
Code format	10 bit binary 8 bit BCD
Temperature range	−20°C to +125°C (Specification) −55°C to +125°C (Operating)

An A/D configuration is shown by Figure 10. The performance parameters are:

I.C. A/D Performance Parameters

Put-through rate	DC to 50K words/sec (10 Bit Binary Accuracy)
Resolution	10 bits (Binary)
Accuracy	±0.05% F.S. (non-linearity) ±0.01% F.S/DAY (fullscale drift @ 25°C) ±0.005% F.S/°C (fullscale drift with temp)

Analog range	Variable, 0 to +12 volts (max.)
Analog input impedance	>1 megohm
Reference voltage	Internal with external trim optional
Logic Control Levels	"1" less than +0.5VDC "0" greater than +2.5VDC
Code format	10 Bit Binary 8 Bit BCD
Temperature range	−20°C to +125°C (Specification) −55°C to +125°C (Operating)

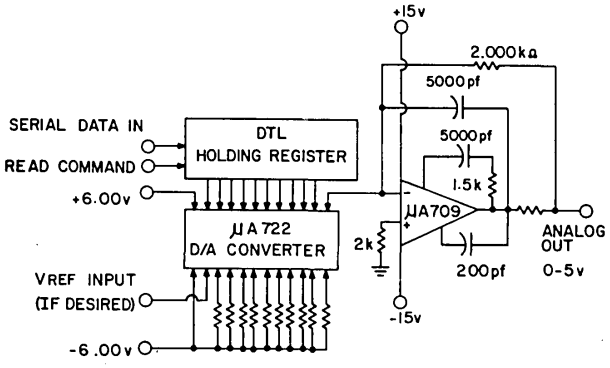

Figure 9—D/A converter

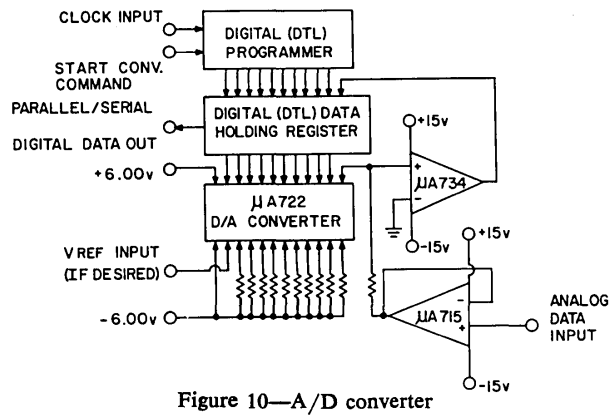

Figure 10—A/D converter

The resistor arrays used in two applications were discrete metal wire-wound devices. Film resistor (thin or thick) may be used, as the array values may be pre-selected to achieve the accuracies stated. If trimmed arrays to match the current sources are desired, the non-linearity error can be reduced to zero at +25°C. Also the components are small enough to easily fit within a P.C. board-mounted proportional control oven. These would allow paralleling units for greater accuracies and 13-15 bit resolution.

CONCLUSION

New IC functional blocks permitting all I.C. analog digital data converters are now nearing production. As with I.C. logic elements, the cost to the user can be expected to fall to the point where economies will grossly change design philosophies in the data acquisition field. These do-it-yourself components will make low-cost analog/digital peripheral subsystems a true reality.

REFERENCES

1 A K SUSSKIND
Notes on analog-digital conversion techniques
The Technology Press MIT and John Wiley & Son Inc Chap 5 1957

2 K HINRICHS
Digital to analog conversion equipments and techniques
1964 Systems Engineering Conference New York N.Y. June 1964

3 B D SMITH
Coding by feedback methods
Proc IRE vol 41 no 2 pp 1053-1058 August 1953

4 M B RUDIN R L O'DAY R T JENKINS
System circuit device considerations in the design and development of a D/A and A/D integrated circuits family
1967 International Solid State Circuits Conference University of Pennsylvania February 1967

5 C T SAH
Effect of surface recombination and channels on p-n junction ana transistor characteristics
IRE Transactions on Electron Devices pp 94-103 January 1962