The IADIC: a hybrid computing element

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INTRODUCTION

One of the major problems encountered in a hybrid computing facility is interfacing the analog and digital copartners. The papers of Hagan and Treiber,[1] Rubin,[2] and Chapelle[3] demonstrate the versatility of the MDAC (Multiplying Digital to Analog Converter) as an interface element.

The MDAC is a hybrid computing element utilizing analog and digital inputs to produce an analog output. The purpose of this paper is to introduce a hybrid analog to digital converter which the authors have named "IADIC" for "Integrating Analog to Digital Converter." The IADIC concept was introduced by Jarret[4] in 1960 but has apparently not received adequate attention. As the name implies, the IADIC integrates an analog voltage and produces a digital output. Integration is performed by a conventional analog integrator with its inherent advantages of speed and continuity. The integrated output is accumulated digitally thereby eliminating the resolution problem inherent in analog computation. To summarize, the IADIC can provide real time, continuous integration with digital precision. These characteristics are very desirable in hybrid guidance and control simulations where high frequency control variables are usually integrated in the analog domain and converted to digital representation for high precision guidance and trajectory calculations.

In conclusion, the error analyses of Jarret[4] and section IV of this paper indicate that as an integrator the IADIC accuracy should be at least as good as the better analog integrators.

I. Theory of operation

A. Description

An IADIC has been mechanized in Figure 1 by combining an analog integrator, comparators, logic, switches, and an up-down counter. When this IADIC is in the operate mode, the scaled integral of the input $\left(\frac{X(t)}{q}\right)$ will be generated as an output and will be represented as a digital count in an up-down counter. When the IADIC (see Figure 1) is in the operate mode, the analog input $-\dot{X}(t)$ is integrated until the integral exceeds either the plus or minus comparator (quantum) level. When this occurs, the logic element gates one of the constant width clock pulses into one of the normally open switches S_1 or S_2. By closing the proper switch for an accurately-known small time, a square wave feedback pulse of opposite polarity to $-\dot{X}(t)$ is generated. The amplitude and width of the feedback pulses are adjusted so that the integral of one pulse is exactly equal to one quantum. Thus the effect of a feedback pulse is to return the integrator output to zero. Simultaneously with the feedback pulse, a count pulse is sent to the up-down counter. An up or down count is sent, depending on which comparator has been violated. The final step in the IADIC operation is to multiply the counter content by the quantum value "q," and the result of this multiplication is a digital number representing $X(t)$, the integral of the input. This multiplication is a scaling operation performed in the digital computer.

In review, the IADIC operation may be outlined as follows:

(1) $\dot{X}$ is integrated until X changes by one quantum level.
(2) A feedback pulse, which returns the integrator to zero, is generated.
(3) A count pulse is sent to the up-down counter.
(4) The process is repeated.

Since the IADIC is an analog to digital converter, it must be considered as a quantizer. Susskind[5] defines a quantizer as a device which converts an input which

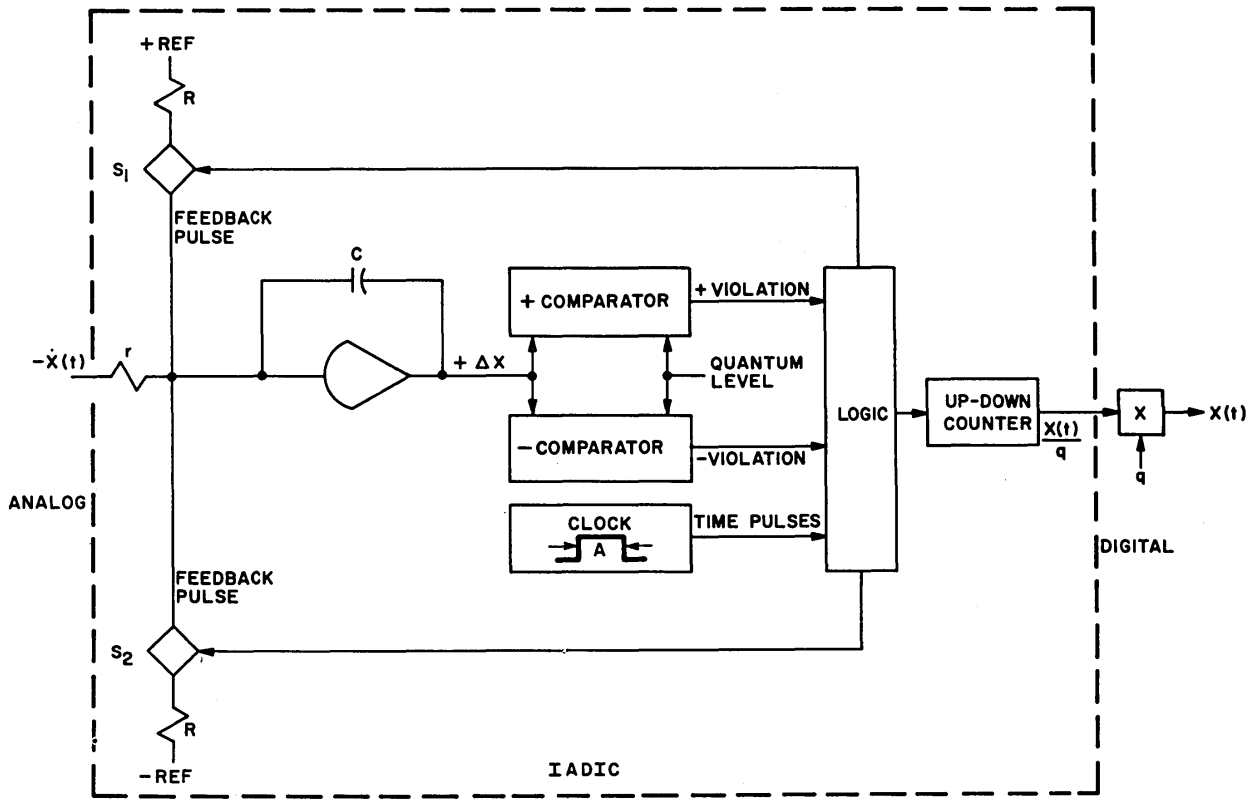

Figure 1—IADIC mechanization

is continuous into an output which has only discrete values. This quantizing action is shown in Figure 2 where q is defined as the quantum level (or quantizing level).

The analog integrator in the IADIC is scaled to ensure that this quantum, q (see Figure 3), will be represented by a reasonable voltage. The output of the IADIC for a step input is shown in Figure 3.

It can be seen by comparing Figures 2 and 3 that the quantizing actions of the IADIC and present analog to digital converters are identical. The IADIC, however, is scaled to represent the least significant bit or quantum level, q, by a reasonably large voltage.

An example will now be developed to clarify the scaling of the IADIC. Referring to Figure 4, the maximum range of $\dot{X}$ will be defined as 500 feet per second; and the quantum level, q, will be defined at 0.5 feet. ΔX, the integrator output, will be scaled for 1.0 foot to allow for overshoot. Figure 1 will now be scaled as shown in Figure 4.

The pulse rate of the clock must be:

$$\text{Pulse rate} = \frac{1}{\Delta T} = \frac{\dot{X}}{q} = \frac{500 \text{ feet per second}}{0.5 \text{ foot per pulse}}$$
$$= 1000 \text{ pulses per second.}$$

Therefore, the waveform for the feedback pulse will be as shown in Figure 5.

The period for the clock pulse, ΔT, is equal to 0.001 second, and the ½ pulse period, $\tau = \frac{1}{2}\,\Delta T$, is equal to 0.0005 second. Now, the IADIC is "reset" by producing a feedback pulse which has an integral equal to a quantum level, or:

$$\int (\text{feedback pulse})\, dt = q$$

$$\frac{1}{RC} \int_{t}^{\tau+t} V\, dt = q$$

$$\text{Thus } q = \frac{V\tau}{RC}$$

If V is assumed to be reference voltage, R (see Figure 1) can now be solved from the above equation:

$$R = \frac{V\tau}{qC} = \frac{100 \text{ x } 0.0005}{0.5 \text{ x } 0.01 \text{ x } 10^{-6}} = 0.1 \text{ x } 10^{6} \text{ ohms.}$$

To reiterate the scaling procedure, the values of r, C, pulse rate, and R are determined as follows:

(1) r and C are chosen to represent q as a reasonable fraction (perhaps ½) of ΔX.

(2) Pulse rate is determined to be $\dot{X}_{max}/q$, or

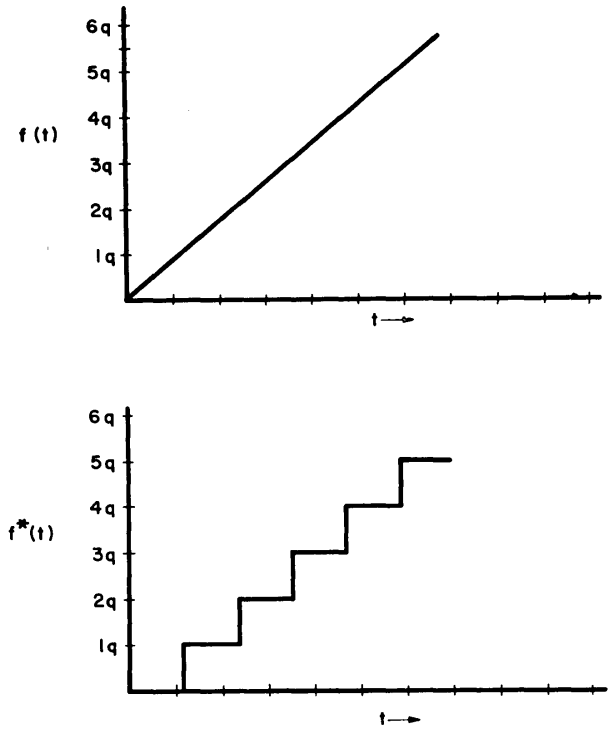

Figure 2—Standard quanitizing action of present analog to digital converters

pulse period, $\triangle T$, equals $q/\dot{X}_{max}$.

(3) R is chosen to make the integral of the feedback pulse, $\frac{V\tau}{CR}$, equal to a quantum level, q (where $\tau = \frac{1}{2}\ \Delta T$). Solving this relationship for R yields the value for R or $R = \frac{V\tau}{qC}$

B. Merits

Before discussing the error sources associated with the IADIC, some of its more obvious merits should be brought to light. These are listed below:

(1) Integration is performed in real time and continuously in the analog domain.
(2) Integration is performed in parallel.
(3) Integration is performed with digital precision (i.e., resolution).
(4) Once the integrator is placed in the operate mode, it stays in operate mode for the duration of the run. Thus no information is lost by going through repeated "Hold" and "Reset" modes.
(5) The integrator output is not limited; therefore, it can exceed the quantum level before, during, or after a feedback pulse, and again no information is lost.

II. Error analysis

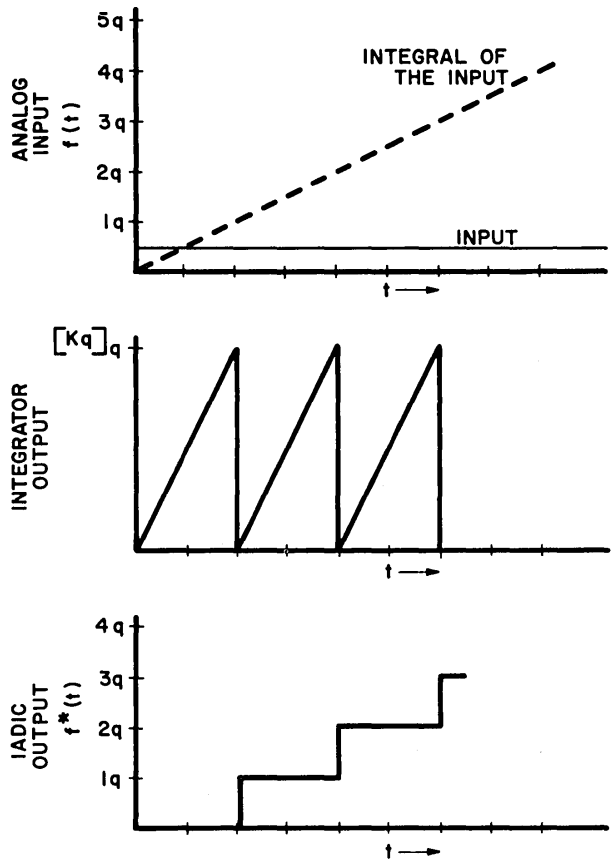

Figure 3—Quantizing action of the IADIC

The following error sources will be considered in this analysis:

(1) An error due to the inaccuracy of the comparators which sense the quantum level q.
(2) An error due to an inaccuracy in the feedback capacitor.
(3) An error in the reset pulse for the integrator.
(4) An error due to the hardware limitations.

It will be shown that the first two errors are canceling or negligible. The significant error sources are reset pulse inaccuracies and hardware limitations.

A. Comparator error

The first error to be evaluated will be comparator inaccuracy; the result of this error is illustrated in Figure 6. The quantum level at which the comparator should change state will be defined as q (see Figure 6), and e will be defined to be an error due to comparator inaccuracy. Therefore, the actual level at which the comparator changes states is q + e. The effect

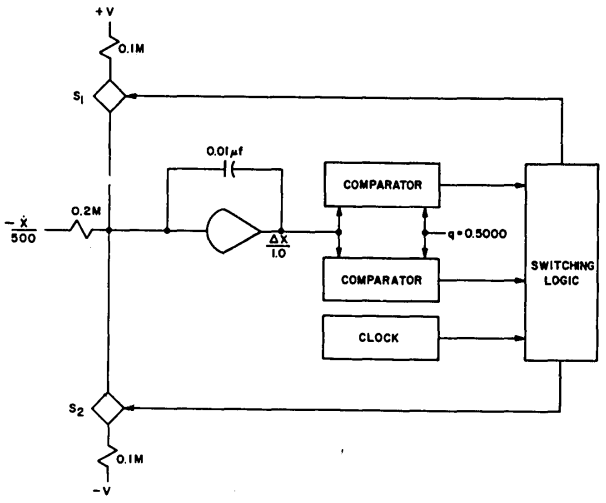

Figure 4—A scaled IADIC

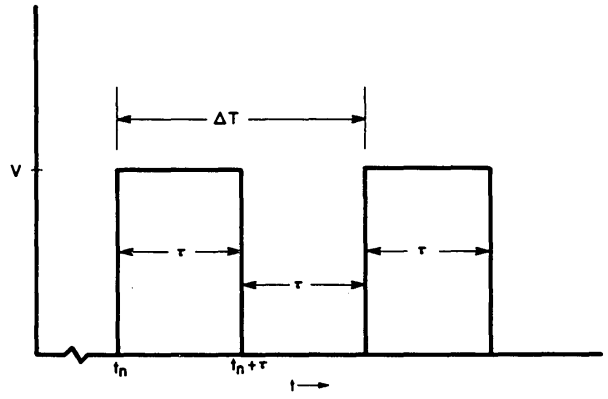

Figure 5—Typical wave shape for a clock pulse

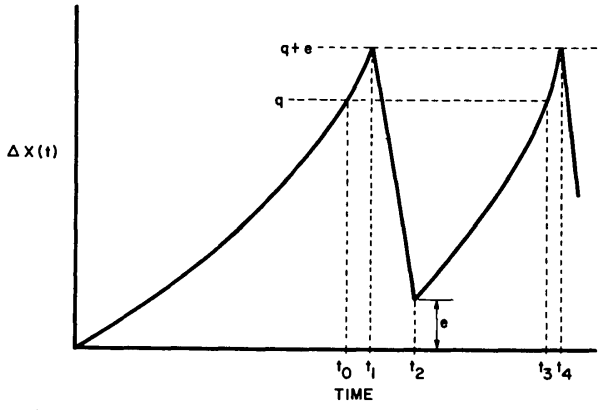

Figure 6—Effect of comparator error

of this error is to cause a feedback pulse to be generated at t_1 instead of t_0 (the proper time), but the feedback pulse will reduce X(t) by the correct value (q), and an error of e will be left on the integrator. On the next cycle (t_2 to t_3), the comparator will trip at q + e. This is a level change of q (not q + e) and produces a new output pulse which is properly interpreted as a change of one quantum (q). Therefore, the integral does contain an error due to the comparator inaccuracy; however, this error does not accumulate and represents only a small percentage of one quantum. The decision to apply a reset pulse to the integrator and not place the integrator in a reset mode condition was predicated on minimizing the effects of this error and the next error to be discussed (feedback capacitor error).

B. Feedback capacitor error

The next error source to be considered is an error in the feedback capacitor. The output of an IADIC with a feedback capacitor error of E is shown in Figure 7. At any time, t, the integrator output can be determined from Figure 7 to be:

(1) Output of integrator at t = output of integrator at t_{i-1} — integral of one reset pulse + integral of input from t_{i-1} to t.
Substituting actual parameters into equation (1) yields:

(2) $$\Delta X(t) = q - (1+E)q + (1+E)\int_{t_{i-1}}^{t} \dot{X}dt.$$

Now, if we let the integrator span the quantum for this interval (i.e., $\Delta X| = q$), equation 2 becomes: t=ti

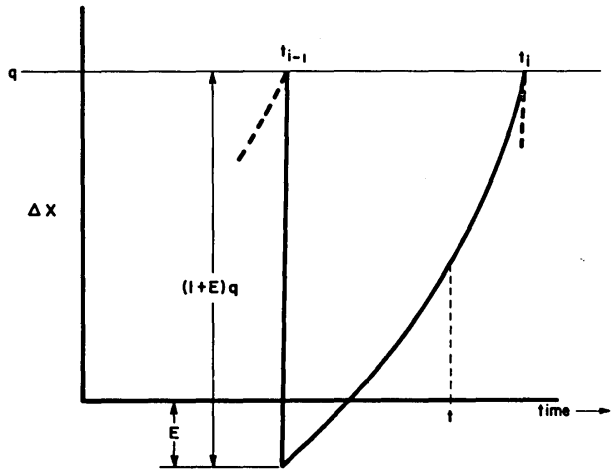

Figure 7—Effect of capacitor error

$$(3)\quad q = q - (1+E)q + (1+E)\int_{t_{i-1}}^{t_i} \dot{X}dt$$

which reduces to:

$$(4)\quad \int_{t_{i-1}}^{t_i} \dot{X}dt = q$$

Although the feedback capacitor was in error by the factor E, the actual value of the $\int_{t_{i-1}}^{t_i} \dot{X}dt$ and the output of the IADIC spanned the quantum (q) in the interval $t_{i-1} \leq t \leq t_i$. Because the input of the IADIC ($\dot{X}$) and the feedback pulse are sensed by this integrator, it is obvious that the first count of the IADIC will have an error due to E, but every subsequent count will be independent of E. The decision to apply a reset pulse to the integrator and not use a reset mode was predicated on reducing the effects of capacitor errors and comparator error.

C. Feedback pulse error

The next source of error to be considered is the accuracy of the feedback pulse. For proper operation, the integral of every pulse must be repeatable, accurately determinable, and equal to q (quantum level). A single feedback pulse as illustrated in Figure 5 will now be considered.

If the integral of this feedback pulse is defined to be q, then:

$$q_n = \int (\text{feedback pulse})\, dt = \frac{1}{RC}\int_{t_n}^{t_n+\tau} V dt$$

$$= \frac{V\tau}{RC} = q$$

where

R = Feedback pulse resistor value (see Figure 1)
C = Integrator capacitor value
V = Reference voltage
τ = Pulse duration.

It has been shown that the capacitor value error does not contribute significantly to the IADIC error. Errors in the reference voltage are insignificant because all measurements are measured relative to the same reference voltage. The two most significant errors are the feedback resistor value and the pulse duration. State of the art summing resistors are adjustable to within ±0.0025 percent; however, the resistance of the switch may be on the order of 50 to 100 ohms, which is a significant error if a 100K feedback pulse resistor is used. Assuming that the feedback resistor can be trimmed to account for switch resistance, then the resistance error would be due to stability of the switch resistance during a run.

The pulse duration is a function of the "turn on" and "turn off" times of the switch. Again, if we assume that the area of the pulse can be calibrated in some fashion, then the actual "turn on" and "turn off" times are not important, but the stability of these times is important. We may now itemize the major contributors to pulse area errors by recognizing that there are three (pulse generator, logic, switch) sources of "turn on" and "turn off" time errors. These major error contributors are as follows:

(1) Switch resistance stability.
(2) Turn on time stability of the pulse generator.
(3) Turn on time stability of the logic circuits.
(4) Turn on time stability of the switch.
(5) Turn off time stability of the pulse generator.
(6) Turn off time stability of the logic circuits.
(7) Turn off time stability of the switch.

The authors were unable to obtain data on these types of errors: however, the required values to obtain reasonable accuracy can be derived. If the IADIC is to be as accurate as a good analog integrator (1.0 μf capacitor), then the feedback pulse area should be accurate to ±0.025 percent.[9] Assuming that this is a one sigma value and that all of the above error sources are independent and equal, then each of the seven error sources may contribute an error of $0.025/\sqrt{7} = 0.00945$ percent to the pulse area. Now assuming a 100K ohm feedback pulse resistor and a nominal pulse width of 10^{-4} second, the required accuracies of the seven error sources in order to obtain 0.025 percent IADIC accuracy are:

(1) Switch resistance stability $= 10^5 \times 9.45 \times 10^{-5}$ $= 9.45$ ohms.
(2) Turn on time stability of pulse generator, logic, and switch $= 10^{-4} \times 9.45 \times 10^{-5} = 9.45$ nanoseconds.
(3) Turn off time stability of pulse generator, logic, and switch $= 10^{-4} \times 9.45 \times 10^{-5} = 9.45$ nanoseconds.

Although the authors were unable to obtain stability data on switch resistance, rise time, and decay time, the required values above do not seem unreasonable to the intuition when one considers nominal values of 50 to 100 ohms for switch resistances and 20 to 40 nanoseconds for rise and decay times.

It should be noted that the expected accuracy of the IADIC will be different for monotonic and nonmonotonic functions. Since independent resistors, switches,

and perhaps logic circuits are used for positive and negative pulses, the error for nonmonotonic functions will be larger by approximately $\sqrt{2}$.

To summarize, the IADIC error is almost entirely due to errors in the feedback pulse area and although little or no data are available to determine this error, a value of 0.025 percent appears to be attainable.

D. Hardware limitations

The decision to provide a resetting feedback pulse and not to reset the mode of the IADIC (see Sections A and B) when a quantum level is reached places severe specifications on the hardware of the IADIC. Because the IADIC may be in operate mode for a long period of time, integrator drift will be detrimental to the accuracy of the IADIC. Therefore, the hardware must be designed to ensure drift-free operation. Also, the hardware must be designed to obtain a feedback pulse with a repeatability which will not degrade the operation of the IADIC. Therefore, to ensure proper operation, the following hardware requirements must be met:

(1) Biases caused by any switch (especially switches S_1 and S_2 — Figure 1) in both the on and off states must be miminized and balanced.

(2) The integrator must be designed to ensure that the integrator rate limiting (due to maximum amplifier current) does not distort the feedback pulse. This rate limiting will affect accuracy and will limit the minimum feedback pulse duration. The amplifier must also be designed to minimize drift.

(3) To obtain quantum equal to a small percentage (10^{-6} percent) of the variable either the comparator levels must be set low or the integrator gain must be high (or both). As the integrator gain is increased, the probability of obtaining drift-free operation will decrease. Thus, the requirement to obtain drift-free operation will place a limitation on the maximum integrator gain, and comparator setting accuracy will place a limit on the minimum integrator gain.

(4) Switches S1 and S2 must have "turn on" and "turn off" times repeatable to 9.45 nanoseconds. To obtain this repeatability the nominal switch time should be on the order of 50 to 100 nanoseconds. Thus the current to be switched must be limited, which places a restriction on the minimum value of R and therefore the minimum quantum level.

(5) Dow,[6] Howe,[7] and Driban[8] have presented discussions on the effect of capacitor dielectric absorption on the accuracy of analog integrators. The circuit to compensate for dielectric absorption developed by Driban[8] could be incorporated into the design of the IADIC to eliminate this dielectric absorption effect.

IV. Analog to digital interface

Getting the count pulses from the IADIC into the digital computer is an infinitesimal problem compared to the normal method of analog to digital conversions which requires: (1) analog sample and hold, (2) multiplexing, and (3) analog to digital conversion. The result of this conversion is a digital number which has to be inputted to the digital computer.

Several schemes were conceived to accomplish the task of getting the count pulses from the IADIC into the digital computer. The final method for imputting the count pulses was to count and store these pulses in a special buffer register. A bank of such registers would be designed into the digital computer. This method excites the imagination because a direct line of communication is established between the analog and digital computers and emphasizes the phrase "copartners in computation."

V. CONCLUSION

Several papers[1,2,3] have been written which tend to validate the proposition that a hybrid computing element is the optimum device to interface an analog computer with a digital computer, but the authors of these papers are primarily concerned with digital to analog communication utilizing the MDAC (Multiplying Digital to Analog Converter). The hybrid computing element (IADIC) introduced in this paper should provide the flexibility and versatility to analog-to-digital conversions that the MDAC provides to digital analog conversion.

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