

Figure 2. Wall Effect.

making it even harder for replacement fluid to flow into the low-pressure region, and eventually lock onto the wall altogether, forming what is called a low-pressure bubble upstream from the point of attachment. This wall effect is sometimes called the Coanda effect.³ Both wall effect and momentum transfer are usually involved in most fluid amplifiers.

The Harry Diamond Laboratories' amplifier, shown in Figure 3, consists of a power jet, A, an interaction region, B, two control jets, C and D, and two output passages, E and F.

The amplifier may be made to operate either proportionally or in a digital fashion, depending on slight differences in geometry. In the proportional device, fluid issuing from jet A will divide almost equally between output passages E and F in the absence of any control signals at C or D; but if a small amount of fluid is blown into the device through control port C, the main jet will be deflected to the right, and more of it will exit from passage F than from

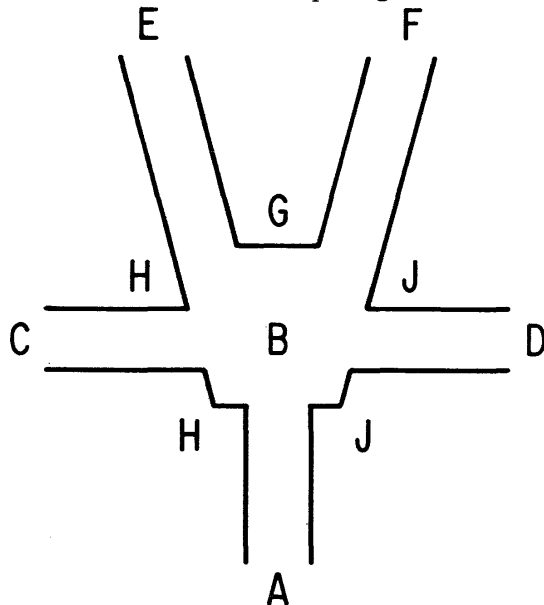


Figure 3. Representation of Amplifier Developed at Harry Diamond Laboratories.

passage E. For small signals, the output variation can be made fairly linear with respect to the input, and furthermore, the output variation will be larger than the input variation, thus producing gain or amplification.

If certain changes are made in the geometry of the proportional amplifier, namely, if the divider tip G is moved further downstream and if the walls HH and JJ are moved closer to the centerline of symmetry, the amplifier becomes bistable or digital. That is, the power jet bends by itself and attaches to one or the other of the sidewalls so that even in the absence of any control signal, substantially all the flow is from a single output passage, for example, passage E.

Assuming an output from passage E, if the pressure at control port C is now slowly increased, no change occurs until a certain threshold value is reached, at which point the power jet suddenly switches to the other side and exits from output passage F. If the control signal is returned to zero, the power jet remains locked to wall JJ and continues to issue from output passage F. Thus, the device has memory capability and is the logical equivalent of the electronic flip-flop.

All the other fundamental switching and logic functions which are now performed electronically can also be implemented by pure fluid devices. Figure 4 shows a pure fluid inverter. This device is purposely made very asymmetrical so that in the absence of a control signal the fluid flows essentially in a straight line and exits from the left-hand leg. Only when a control signal of sufficient strength is present will the jet be blown over to the right-hand leg. The wall lock-on effect on the right-hand leg is minimized, and when the control signal disappears the output will immediately return to the left-hand leg. Thus, the output from the left-hand leg is the inverse of the control signal; the output from the right-hand leg is the control signal amplified.

An OR gate may be readily constructed by converting the pressure energy in two or more signals to velocity energy and directing this into a common receiver, as is shown in Figure 5. Because of the vector quality of the two jets, there will be very little leakage of signal from

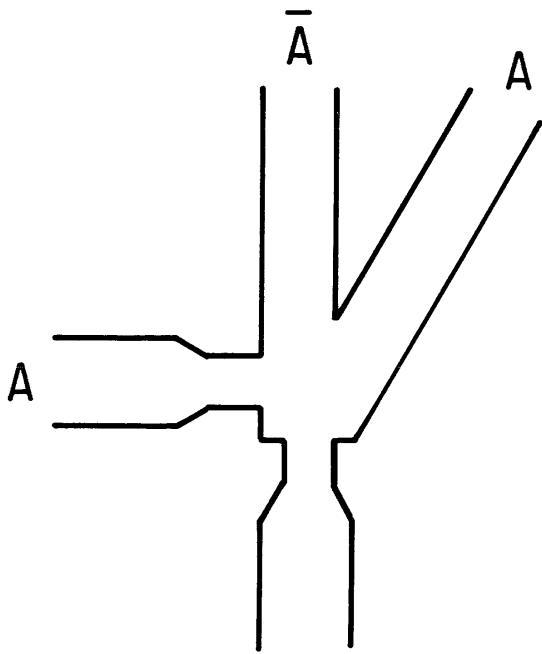


Figure 4. Inverter.

one input backward through the other unless the output is substantially blocked, in which case the fluid would have no place else to go. The purpose of the two side passages shown in Figure 5 is to provide for fluid escape in just this eventuality. If a high impedance is presented to the output the fluid will escape through the side bleeds rather than reversing and flowing into the other signal input.

The vector properties of high-velocity jets are also made use of in the AND gate (Figure 6). If the signal A is present alone it will pass straight through the AND gate and vent to atmosphere, and similarly for B alone. If signals A and B are present simultaneously, however, and have approximately equal amplitudes, then the resulting jet will make an angle of 45° to the original jets and will be caught in the receiver placed at this position. With proper design of the receiver exact balance of the two signals is not necessary. Ratios of 2 : 1 are easily accommodated.

The combination of the OR gate and the inverter as shown in Figure 7 gives an extremely powerful element. The right-hand output is the amplified OR function of the inputs while simultaneously the left-hand output gives the

amplified NOR function, that is, $\bar{A} \cdot \bar{B}$. This principle has been extended to achieve a NOR gate with a fan-in and fan-out of four; that is, the device has been provided with four input terminals. The presence of a signal on any one of these terminals will switch the device off, and the output has been divided and channeled to four output terminals so that four identical elements can be driven from one element. In this NOR gate the OR output is not provided.

As is well known, all logic and switching functions can be implemented with NOR gates alone. A flip-flop, for example, can be made by interconnecting two NOR elements, as is shown in Figure 8.

In this configuration, one element is in the 1 state, and its output is used to switch the other element into the 0 state. The elements remain stable in their respective states until an outside signal changes the state of the flip-flop. With reference to Figure 8, assume that element A is in the 1 state, that is, its output signal is in leg d. This signal is sent to element B through input j which switches the element into the 0 state, that is, the jet is diverted to

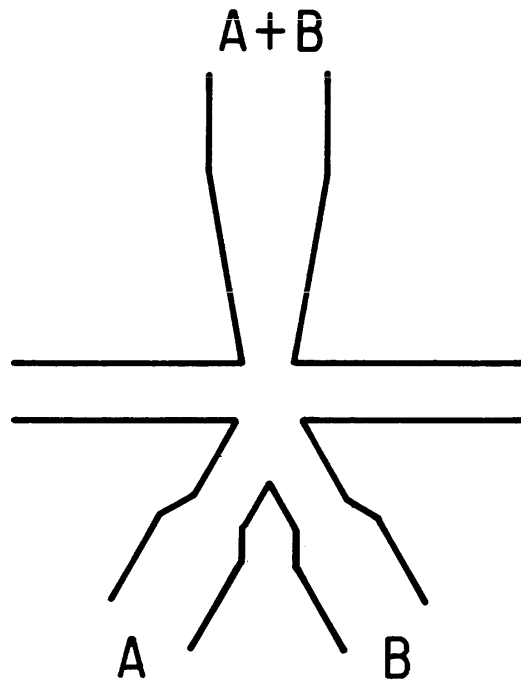


Figure 5. OR Gate.

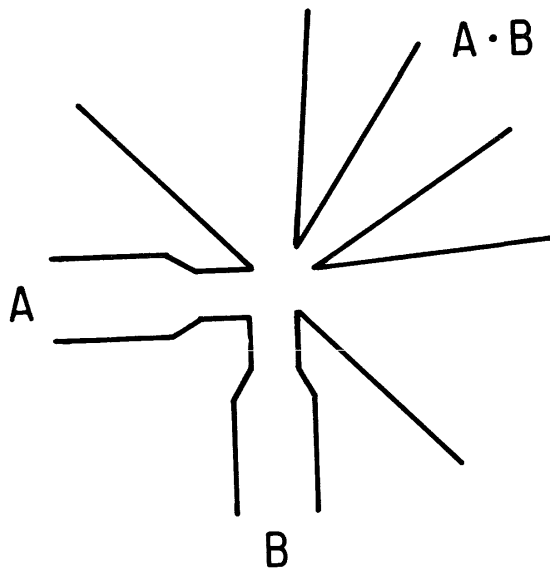


Figure 6. AND Gate.

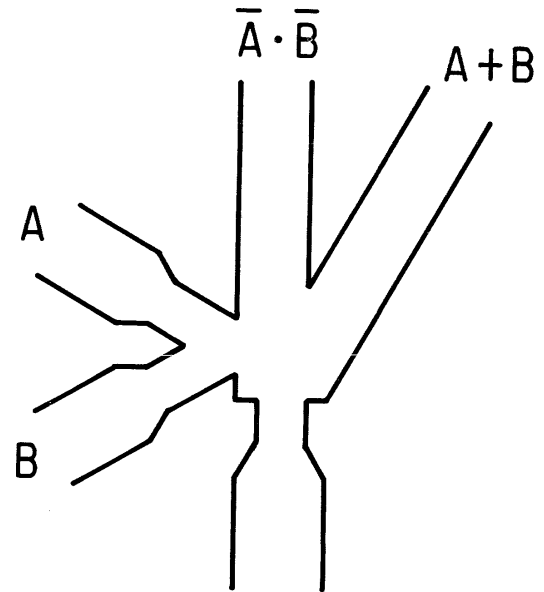


Figure 7. NOR Gate.

output f. There is no signal in leg e of element B; therefore, element A is not affected by element B. The flip-flop will remain stable in this state until an outside signal is applied to element A by way of input h. When the signal appears, A will be switched to the 0 state, and the jet will be diverted from leg d to leg c. The signal to input j of B will go off, and the element will switch from the 0 state to the 1 state, that is, the jet will switch from leg f to leg e. The signal from B will then be applied to A through input g. When the outside signal through h is removed, the signal through g will keep A in the 0 state. The flip-flop has been switched, and it will remain stable in this state until another outside signal is applied to input k of element B.

FLODAC is built entirely of NOR gates and requires about 250 of these elements to do its job. FLODAC, incidentally, stands for Fluid Operated Digital Automatic Computer.

Why Fluid Amplifiers?

Granting the feasibility of constructing complex digital systems from fluid amplifiers, what is the motivation for doing so? What advantages, if any, do fluid amplifiers have over their well-established electronic counterparts? The use of fluid amplifiers rather than their electronic counterparts may be justified on the

basis of four significant advantages: reliability, environmental immunity, low cost, and absence of r-f radiation. Each of these advantages is briefly discussed below:

1. *Reliability:* Pure fluid amplifiers have no moving parts except the fluid itself. There is nothing to wear out, nothing to age, nothing to burn out. With the proper selection of structural material and fluid, there are no potential chemical or solid-

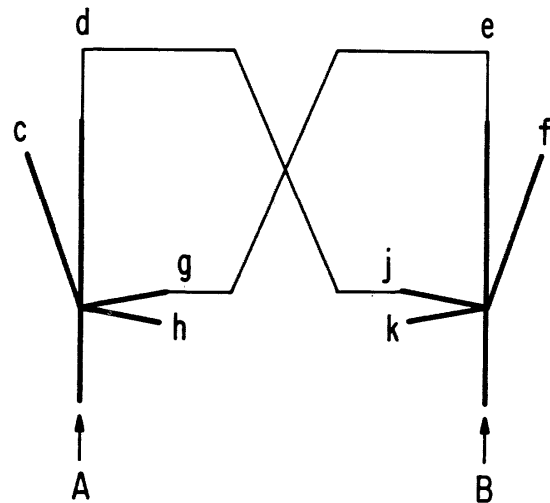


Figure 8. FLODAC Flip-Flop.

state reactions. There need be no delicate structures. In short, the life of a fluid amplifier should be practically infinite, whether in use or quiescent. About the only conceivable cause of deterioration would be dirt in the fluid, and this can be controlled easily by filtration and the use of closed-cycle systems.

The fluid amplifier art is still too young for masses of statistical data on reliability to have been compiled. However, the nature and operation of these devices are such that extremely favorable comparisons with electronic and other types of devices can be expected.⁴

2. *Environmental Immunity:* Fluid amplifiers can be made of almost any solid material, for example, plastics, metals, glass, or ceramics. If the right materials are selected, operation is possible under environmental conditions which preclude the use of electronic devices. For example, ceramic fluid amplifiers could operate at white heat. Metal fluid amplifiers should be operable in intense radiation fields. With the proper materials and assembly procedures, shocks, or accelerations, of thousands of G's should present no problem.
3. *Low Cost:* Fluid amplifiers consist basically of rectangular channels in a suitable material. They can be fabricated by any one of a number of extremely low-cost methods, such as casting, injection molding, stamping, or etching. Entire circuits of fluid amplifiers, including the interconnecting passageways, can be formed by such methods in one low-cost operation. Planes could be stacked one on top of another with holes in the planes at the proper locations for the necessary interconnections. With techniques such as these, which are already being developed, it is estimated that the cost of fluid amplifier circuits may be as much as 100 times less than the cost of comparable electronic circuits.
4. *R-f Radiation:* No electromagnetic energy is radiated by fluid circuits; consequently, a very common and often serious problem associated with electronic logic, namely,

r-f radiation, is eliminated. Often extensive and costly measures must be taken to shield electronic equipment to prevent interference with other equipment or communications or to prevent detection of radiated intelligence by hostile agencies. However, such measures are never 100 percent effective. Also, external radiation can seriously affect electronic equipment by causing errors or malfunctions. Both of these problems are completely eliminated by fluid devices, which neither emit nor are affected by radiation.

Operational Speed

Fluid amplifiers have one significant disadvantage: their operational speed is relatively slow. Switching times are of the order of a millisecond, and signal propagation time is of the order of a millisecond per foot. Fluid amplifiers, at present, are only approaching kilocycle rates of operation as opposed to the megacycle and higher rates common in electronic systems. Speeds can be expected to improve, of course, but nanosecond switching times are not foreseeable today. Because of this speed limitation, there may be applications where fluid amplifiers are not suitable.

It should be noted that the inherent speed limitation can be offset appreciably by taking advantage of the low cost and high reliability of fluid amplifiers, which make it economical to compensate for much of the speed deficit by making extensive use of parallel and polymorphic operation.

In any event, there are numerous applications where the speed of fluid circuitry is adequate. Today's system designer must realize both the merits and shortcomings of these new elements; by appraising his problem requirements objectively, he can use fluid amplifiers with excellent results wherever their advantages enable them to do the job better and/or more economically.

SPECIFICATIONS AND LOGICAL DESIGN

Every general-purpose digital computer must have means for accomplishing four basic functions: Memory, Arithmetic, Control, and Input/Output. Consequently, it was necessary to provide these functions if we were to fully meet the goal of demonstrating a generalized fluid com-

puter, even though on a very small scale. All four functions are fully and formally developed in FLODAC.

The problems of memory size, word size, and instruction set are all interrelated. The objective was to build a very small air-powered general-purpose digital computer which could be programmed to do a few elementary problems. At least three instructions seemed necessary to prove generality: an Arithmetic instruction, a Data Transfer instruction, and a Conditional Jump instruction. Since two bits are needed to specify three instructions, a fourth instruction becomes possible without any increase in word size. It was decided to make this a Halt instruction. The four instructions used then are:

Instruction	Code	Explanation
Transfer	T m	10 (A) → m
Add	A m	11 (m) + (A) → A
Jump	J n	01 Go to instruction in memory location n if (A) ≠ 0; otherwise continue with the next instruction in the memory.
Halt	H	00 Stop the computer.

After a few trials it was found that a reasonable program could be written using all four instructions with a memory of only *four words*. This program, which is the basic test program for FLODAC, will be discussed later.

A four-word memory implies two bits for addressing, and this, with the two bit operation code, fixes the word length at four bits. The first two bits of a word are the operation code and the last two the address. Alternately, a word may consist of numerical data only.

To recapitulate, FLODAC has four instructions and four words of memory; each word is four bits long. To compensate as much as possible for the speed disadvantage of fluid elements, operation is bit parallel.

Figure 9 shows the overall block diagram of FLODAC. Each instruction is processed in four steps by the step counter which is driven from the master clock. The control counter contains the address of the next instruction to

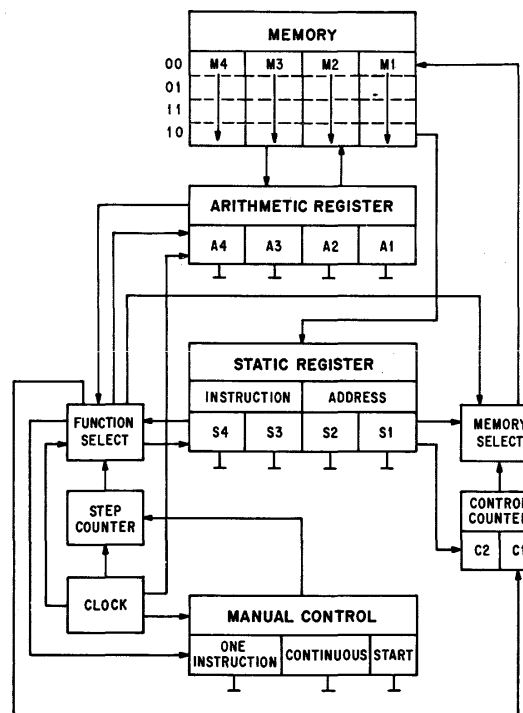


Figure 9. FLODAC, Block Diagram.

be executed and, except during the fulfillment of the Conditional Jump instruction, is augmented by one at the end of each instruction cycle. During step 1 the control counter operates the memory select circuits, and by the end of step 1 the specified memory word, which contains the next instruction, is read into the static register. The two left-hand bits are decoded as to operation, and this information is sent to the function select circuits, where, in conjunction with step counter and clock signals, the necessary gating pulses for all instructions are generated. The two right-hand bits, specifying the operand address, are sent to the memory select circuits, permitting the required data word to be read out. All this takes place during step 1. The actual instruction execution is carried out during some or all of the last three steps.

The Add instruction is carried out in two stages. The first stage is completed during step 3 and consists of adding the word in the memory to the word in the arithmetic register without regard to carry. This portion of the Add instruction changes a bit in the arithmetic register from a 1 to 0 or vice versa, whenever there

is a 1 in the corresponding position of the word to be added. The second stage of the addition process starts at the beginning of step 4 and causes a carry pulse to be sent to the next more significant bit position wherever the sum bit is presently a zero and the addend bit was a one. Means are provided to rapidly transmit the carries to subsequent stages if the original carry pulse would in turn produce another carry at the next higher bit position. This carry generation and propagation proceeds asynchronously and could continue during steps 4 and 1, if necessary. It is actually completed by the end of step 4.

A brief description of the operation of the memory may be in order here. The memory is

a two-dimensional matrix array using flip-flops as the storage means.

Figure 10 is a schematic of the FLODAC memory. Each block represents a NOR element with four inputs and four outputs. Lines into the left side and bottom of the blocks indicate inputs to the elements, and lines from the right side and top represent outputs from the elements. The memory contains four words, each consisting of four bits of information. The words are located in vertical columns, the right column being the first or 00 word address. The horizontal rows contain the same information bit for all four words, the top row being the least significant bit.

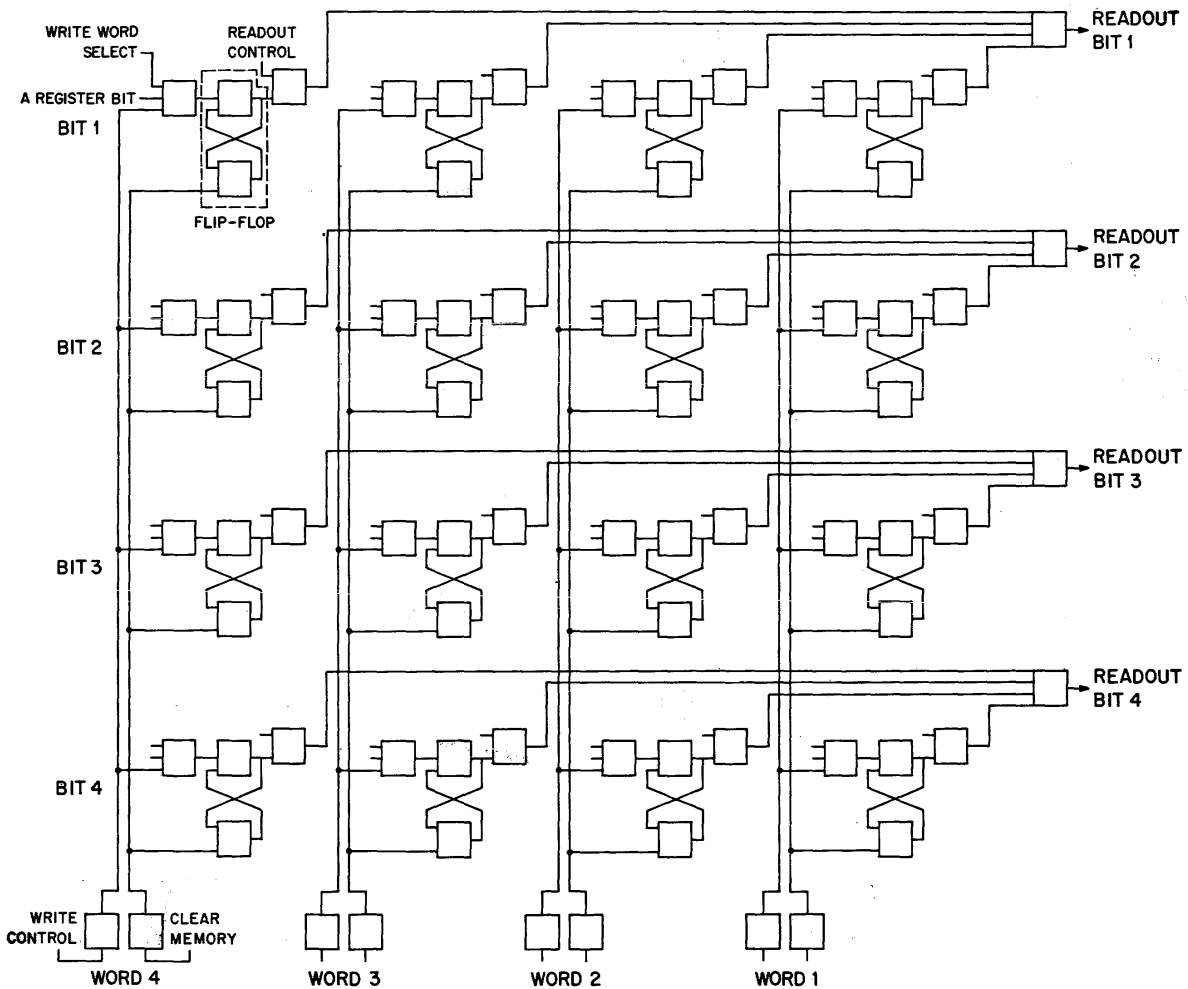


Figure 10. FLODAC Memory, Schematic Diagram.

Writing into memory is a three-step operation. First, the memory storage location is selected by the static register and the memory select circuits. Second, a clear memory signal from the function select erases any information already in that word location by resetting all flip-flops to zero. Third, the word in the accumulator is gated into the memory location by another function select signal. The write operation utilizes three counts of the step counter cycle.

A simple nondestructive readout is employed. Each of the 16 memory flip-flops feeds into an intermediate NOR element which in turn sends a signal to one of the four memory readout elements (far right in schematic). These intermediate elements are controlled by the memory select circuits. When a particular address is chosen for readout, the memory select turns off the intermediate elements of the other three words, thus prohibiting any output signals from these words. Parallel operation is used. Therefore, all bits of a word are written into and read out simultaneously.

Referring back to the overall block diagram, Figure 9, it is seen that a manual control unit is provided which makes possible two modes of operation: *continuous* and *one instruction*. To enter information into the memory of FLODAC the computer is placed in the *one instruction* mode. A word is then set up manually in the A register, and a Transfer instruction specifying the desired memory location of the word is set up in the static register. When the START switch, also located in the manual control unit, is activated, the word in the A register will be transferred into the memory. This process is repeated for each word to be loaded. It should be mentioned perhaps that the act of setting a switch consists merely in putting one's finger lightly over a bleed hole on the control console (Figure 11). The resulting back pressure will then set a flip-flop or generate a fluid pulse, as

the case may be. It is difficult to imagine a simpler form of keyboard. The contents of the A register and static register are displayed by using bipositional visual indicators. The indicators consist of a colored ball in a glass tube. The balls are lifted into view by a pressure signal when the flip-flops are in the 1 state.

CONSTRUCTION AND TEST

Production of Logical Elements

The NOR elements used in FLODAC were made by injection-molding a thermoplastic material into a metal negative master.

The physical size of the fluid devices is a function of the width of the power input nozzles. The widths of the nozzles used on the FLODAC elements were either 0.016 inch or 0.020 inch. These widths were chosen because they allowed the use of standard laboratory fabrication techniques and equipment and afforded accessible tolerances. Increased dimensional accuracy was obtained by machining the master from a large template five times normal size and reducing by means of a pantomill.

Reducing the size of the elements with the above fabrication method is limited by the size of the cutting tool used in making the master. A nozzle width of 0.005 inch might be attainable, but present photoetching processes are able to produce still smaller and more accurate models.

Testing the Individual Elements

Because of dimensional variations occurring during fabrication, the characteristics of the elements sometimes differed. It was necessary, therefore, to set up a testing procedure to check out all elements before using them in the FLODAC circuits. Two testing criteria were chosen. The first was that the pressure recovery be at least a set minimum value. Pressure recovery is the ratio, expressed in percentage,

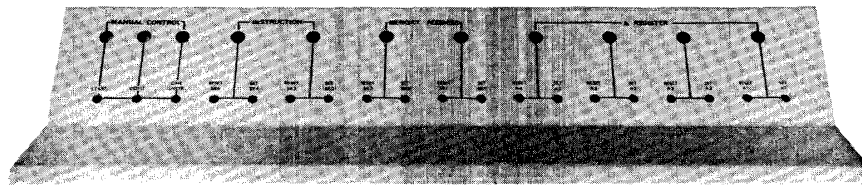


Figure 11. Control Console.

of the output pressure to the input supply pressure. At the present state-of-the-art, the NOR elements have a rather low pressure recovery factor. The FLODAC elements averaged about 30 percent, although other experimental models have reached almost 50 percent. Acceptability for FLODAC required a pressure recovery of at least 28 percent.

The second test for the elements was gain. This is the ratio of the element output to the input signal required to switch the element. A figure of 1.6 was chosen as the criterion here. The supply pressure for the elements in FLODAC was 20 inches of water (0.8 of a pound per square inch). This means that the output pressure would have to be at least five inches of water and that the elements would have to switch with less than three inches of water input signal pressure. Elements not meeting these specifications were rejected. All tests were made with the device loaded with the equivalent load of four other elements.

Method of Assembly and Testing of Circuits

To simplify construction and testing of FLODAC, the computer was divided into two parts. Each half consists of a power supply manifold and three rows of NOR elements. There is a total of 280 elements in FLODAC. The existing circuitry requires only 250 NOR elements, but the extra elements were added in case replacements had to be made or for possible changes or extensions to the logic. The NOR element power inputs are plugged directly into the manifold. Interconnection of the elements is done by simply connecting one of the four outputs of an element to one of the four inputs of the next logical element in the circuit. These connections were made with plastic tubing.

One side of the computer contains the clock, step counter, instruction portion of the static register, function table, and A register circuits; the other side contains the control counter, address portion of static register, memory select, and memory circuits.

The two halves were wired and tested independently. Simulated pressure signals were used where necessary when testing the circuits on each side. When both were working separately, the entire computer was assembled, all the cross connections between the two sections

were made, and appropriate outputs were connected to the control panel indicators. To facilitate maintenance, FLODAC was constructed so that one side hinges out, exposing all of the internal circuitry (Figure 12).

The entire system was then tested, and after straightening out a few minor problems in the circuitry, FLODAC was working reliably as an independent, coordinated system. Figure 13 is an overall view of the finished FLODAC assembly.

Testing the Complete Computer

After all the elements had been interconnected, the system was ready for a complete checkout. This was done by carrying out simple programs which required use of the four computer instructions: Add, Transfer, Jump, and Halt. Instructions were stored in the four-word, four-bit memory unit.

The FLODAC clock was capable of being pulsed manually so that a program could be carried out one step at a time and checked for correctness at every intermediate step. Pressure taps connected to indicator manometers were placed at critical points throughout the computer circuitry. This showed the state of the elements and greatly simplified troubleshooting.

When a program was working satisfactorily with manual clock control, the program was tried with automatic computer controls. In-

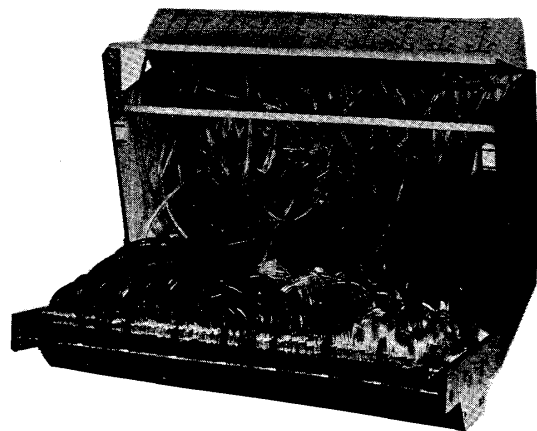


Figure 12. FLODAC Circuitry, Internal View.

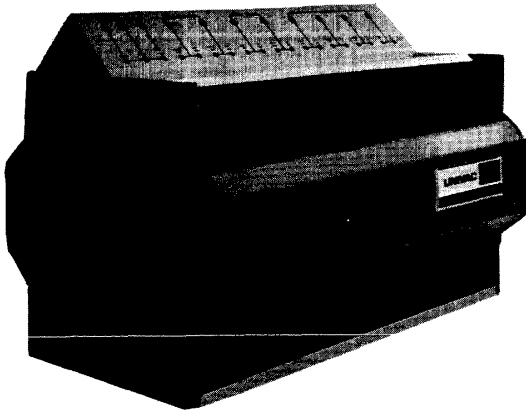


Figure 13. FLODAC.

formation was stored in the memory, the process was started by manually pressing the program START button, and the program was carried out automatically.

The most comprehensive test program makes use of all four instructions and is shown below as a matter of interest.

Memory

Location	Instruction	Address	Explanation
1	A	4	$(4) + (A) \rightarrow A$
2	T	4	$(A) \rightarrow 4$
3	J	1	Go to location 1 if $(A) \neq 0000$; otherwise go to location 4.
4	xx	xx	Arbitrary number; or Halt instruction if 0000.

This program takes an arbitrary number (stored in memory location 4), adds it to the accumulator, transfers the sum back to memory location 4, tests to see if the number in the accumulator is now zero, and repeats this process automatically until the sum in the accumulator is zero. When this condition is reached, as it must be after at most five cycles, the Conditional Jump back to 1, stored in memory location 3, is not carried out, and the program moves on to memory location 4. The content of memory location 4 is now 0000, which is interpreted as a Halt instruction, and the computer stops. The above program, of course, doubles

the number in the accumulator on each cycle after the first.

Alternately, memory locations 2 and 3 can be interchanged, and in this case the accumulator will be augmented each cycle by the number initially stored in location 4 until it again reaches zero. In this form 16 cycles are possible.

SUMMARY AND CONCLUSIONS

The individual reliability test given to each component NOR element greatly reduced the probability of encountering any serious problems during the final checkout of the system. A few minor logic and performance problems did show up, but these were easily traced and corrected. FLODAC was operating reliably only a few weeks after construction was begun.

The nominal clock rate of FLODAC is ten cycles per second. This was chosen to avoid wave propagation and reflection problems which are potential dangers at not very much higher frequencies because of the long lead lengths involved and the lack of attention given to exact impedance matching. It should be pointed out that the speed of fluid signal propagation in air is almost one million times slower than the speed of signal propagation in electric wires. Thus, from the point of view of signal wave length, a frequency of ten cycles per second using air as the working medium is analogous to a frequency of ten megacycles in electronics. Simpler circuits built with elements identical with those in FLODAC, but compactly packaged, have operated with clock frequencies as high as 250 cycles per second.

FLODAC has amply demonstrated that a pure fluid general-purpose digital computer is indeed feasible. The question remains: Is such a computer desirable? There are many areas in which fluid logic cannot hope to compete with electronic logic simply because of the speed limitations inherent in fluid systems even if the utmost advantage is taken of parallel and polymorphic operation.

Conversely, however, there are areas involving extreme environments, such as very high radiation levels or very high temperatures, where present-day electronics cannot hope to compete with fluids, and here fluid logic may

supply the only means of solving many pressing military and space science problems. Between these two extremes there is a vast area where fluid logic does appear to be competitive with electronics and where the advantages and disadvantages of both approaches will have to be carefully studied. This area includes such devices as adding machines, desk calculators, tabulating machines, process control computers, and such peripherals as keyboards and punched card and paper tape readers. Here, timing rates are frequently below a kilocycle, and the speed disadvantage of fluid amplifiers disappears. Here too, the tremendous cost advantage plus the postulated reliability advantage makes fluid logic look very attractive indeed. It may further develop that, given sufficient cost and reliability advantages, the marketplace may well learn to live with slower computing speeds for small general-purpose computers.

The authors believe that there is a vast role to be played by fluid technology in the computer field, and this view is shared by their company.

UNIVAC's FLODAC is the precursor of what we hope will be long series of useful pure fluid systems of increasing complexity and decreasing cost.

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DESIGN AUTOMATION UTILIZING A MODIFIED POLISH NOTATION

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INTRODUCTION

Our first objective in developing the Design Automation (DA) System described herein was to produce and maintain, using a digital computer, the manufacturing and field service documents for a small electronic calculator. However, as a long range objective we wanted a system capable of handling the documentation for virtually any digital computing device, and aiding in certain design functions. On the surface this appears to be the very task performed by existing DA systems but as it turns out the construction techniques used on the calculator give rise to problems not normally handled by these systems.

Because of the wide variance between existing and anticipated construction techniques, it was decided to use Boolean equations as the basic input. The equations are written in a modified form of Polish notation which enables one to very effectively relate the logic to the hardware for trouble shooting purposes. Along with the equations a description of each gate, flip-flop, etc. is input to the system. The form of these descriptions readily accommodates most types of hardware implementation.

This paper is based upon our experience in documenting the design of a small electronic calculator. We shall indicate, as we go, how the system is generalized to handle other digital computing devices.

THE EC/130

To give the reader some idea as to the size of the device we set out to document, we mention here a few of the features of the Friden electronic calculator model EC/130. In addition to those features normally associated with desk calculators the EC/130 (cf. Figure 1) has a four high push down stack as well as auxiliary storage. All stack information is stored on a magnetostrictive sonic delay line and constantly displayed on the cathode ray tube shown in Figure 2.

The EC/130 is a low cost high production item on which great engineering effort has been expended to reduce size and cost to a minimum. As a result of this intense engineering effort the degree of standardization is minimal. No

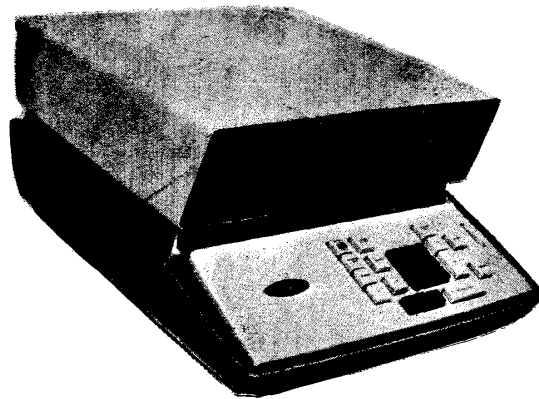


Figure 1. Friden Electronic Calculator Model EC/130.