A NEW TECHNIQUE FOR USING THIN MAGNETIC FILMS AS A PHASE SCRIPT MEMORY ELEMENT

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INTRODUCTION

The use of thin magnetic film memories for high speed computers has been well established. More recently, efforts have been made to adapt thin-film memory elements for operation in a phase script mode by using drive fields at two different frequencies to switch and read the state of the memory element. The resulting memory system is uniquely suited for operation in a parametron computer where information exists as a phase state rather than an amplitude state.

Work by E. Goto at the University of Tokyo,[1] and a disclosure by W. E. Proebster of IBM[2] illustrate some of the techniques proposed. An alternating field, at half the subharmonic frequency of the parametron machine, is applied in the transverse direction. The simultaneous application of an appropriately phased sinusoidal field in the easy direction, at twice the frequency of the transverse field, will cause the magnetic vector to creep to the opposite state, or remain in its initial state, depending on the phase of the easy direction field.

WRITING OPERATION

If two sinusoidal and orthogonal magnetic fields at frequencies f and f/2 are simultaneously applied to the film, the resultant applied field

$$\vec{H} = \vec{H}_{easy} + \vec{H}_{transverse}$$

creates an imbalance that is able to switch the magnetic vector by creeping. Operation in this mode has the inherent limitation that many RF cycles are required to change the state of the magnetic film, resulting in a long write time. This was a major drawback in the "dual-frequency" operation utilizing ferrite cores, although the magnetic principles involved were somewhat different.[3]

It would be desirable to cause $\vec{H}$ to cross the switching threshold in one direction and to remain well below the threshold when it is reversed. This may be accomplished by increasing the amplitude and asymmetry of the transverse field, perhaps by adding some second harmonic in such a way as to cause a flat part on one half cycle and a peak on the other. However, there is still a problem of specifying and controlling tolerances of the creep threshold, as yet a requirement beyond the state of the magnetic film art.

In addition to these problems, there are serious circuit complications with the use of a sinusoidal word field in a dual-frequency memory. An economically feasible system requires some sort of matrix selection scheme for the word lines. Early ferrite core dual-frequency memories[3] required one word driver per word—a prohibitive expense for a large (>1,000 words) memory. A row-column selection system allowing linear select operation would be more desirable. The circuitry to provide sinusoidal word currents for such a matrix is very complex.

A new technique has been developed by the writers which utilizes appropriately timed unipolar pulses applied in the transverse direction. These are at the same rate as the accompanying sinusoidal field applied in the easy direction. This technique has the advantage that the pulses may be shaped and timed (Figure 1) so that the trajectory of the applied H-vector in the H_t-H_e plane has only one crossing point on the switching threshold curve as may be seen from Figure 2. This eliminates undesirable creeping. The obvious additional advantage is that, since only uni-polar pulses are required in the word line, simple row-column selection circuits (commonly used for a linear select memory) are suitable. Since pulses of only one direction are supplied to the word line, only one line isolation diode per word is required.

A major advantage of the new mode is that creep phenomena are not required for writing. Rotational switching occurs within the duration of one uni-polar word pulse. This eliminates one major drawback of previous dual-frequency memories—limited speed writing.

READ OPERATION

For sensing the state of the memory element, only the field in the transverse direction is applied. This operation is similar to that found in conventional film memories. The read field may be the same uni-polar pulse required for writing. On the rise of the transverse field, the magnetic vector rotates clockwise or counterclockwise, depending on the direction of magnetization of the film (Figure 3). On the fall of the field, it returns to its original position. The flux change produces an output signal as in Figures 4a and 4b. It may be seen that,

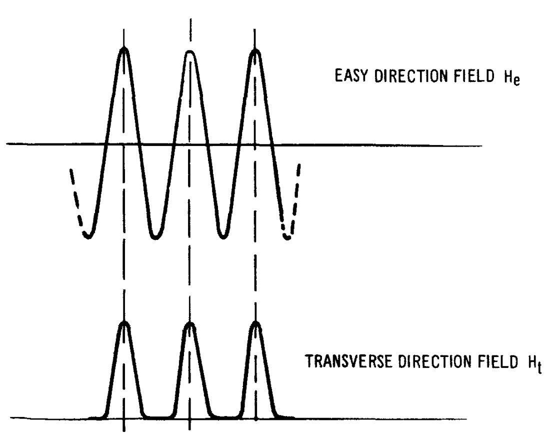

Figure 1. Unipolar H_t Pulse and Sinusoidal H_e.

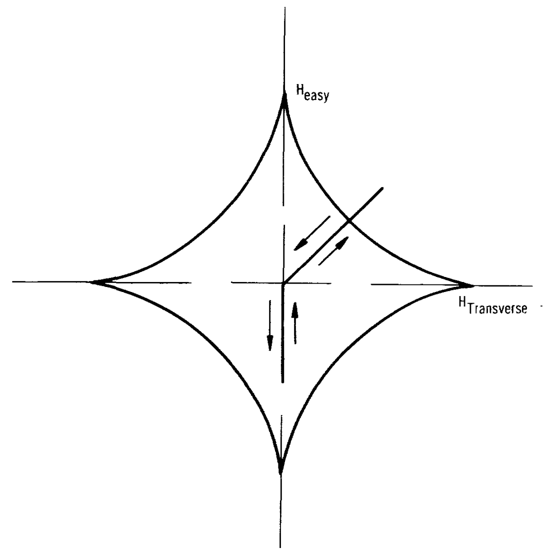

Figure 2. Locus of Applied Field During Write Cycle with Unipolar $\vec{H}_t$.

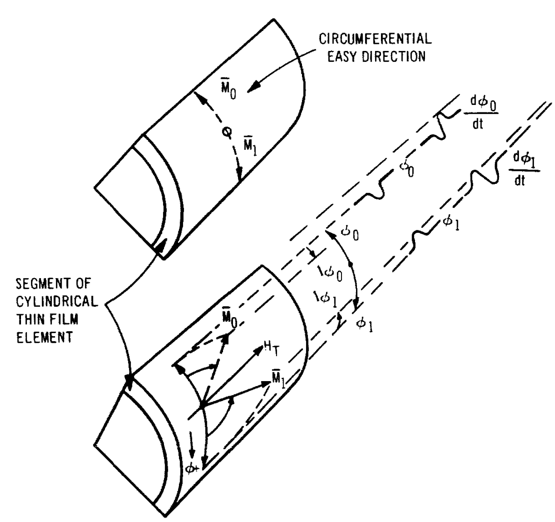

Figure 3. Derivation of Readout Signal.

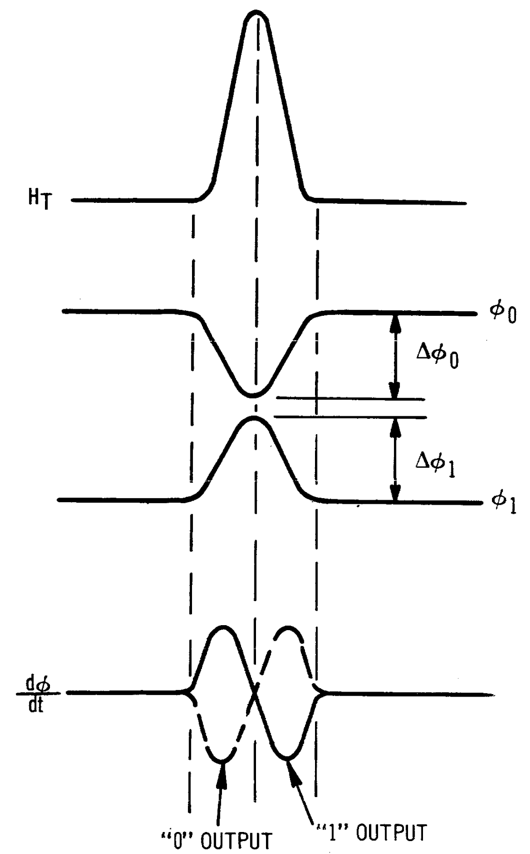

Figure 4a. Readout Signal Waveforms.

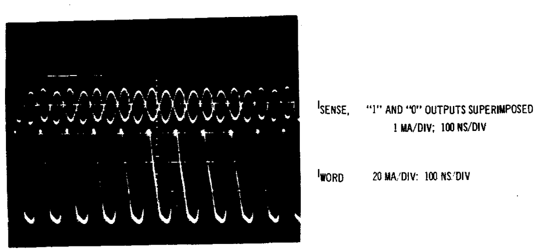

Figure 4b. Phase Script Readout Waveforms.

depending on the state of the film (1 or 0), the two outputs will be mirror images of each other. Since a train of uni-polar pulses is applied for readout, a train of pulse pairs at the same PRF appears on the readout line. It may be readily seen that this waveform contains phase information which may be used to lock a parametron operated as a sense amplifier.

It should be noted that this technique is equally suitable for the various physical forms of thin-film memory elements, i.e., films deposited on cylindrical wires with either an axial or circumferential easy direction, or on a flat film array. It is also noteworthy that this technique of operation preserves the inherent capability for NDRO operation since the read field is applied only in the transverse direction, and if it can be kept below the worst-case creep threshold of the film, nondestructive readout may be obtained.

One design requirement of the memory element is a certain degree of NDRO capability, since a finite time is required to lock a parametron sense amplifier to the desired phase. If creep, due to a transverse field, is possible, it must be such that the output signal is available for a sufficient number of read pulses (typically 10-20) to allow the sense amplifier parametron to lock into the required phase state.

USE OF COMMON PARAMETRON FOR SENSE AMPLIFIER AND DIGIT DRIVER

A major advantage of this type of memory is the potential use of a single parametron for both the sense amplifier and the digit driver. The operation is as follows: the flux change caused by the word current flowing in the word line at read time causes readout signals to appear on the sense line either in "one" phase or "zero" phase. These are then fed by an appropriate matching network to a parametron operating as a sense amplifier. When properly clocked, this readout signal forms the "seed" to lock the sense amplifier parametron and allow it to build up to steady-state with the phase of the readout signal. This parametron may be designed so that it can supply sufficient current into the digit line to automatically rewrite (in conjunction with applied word current which is simultaneously present) the information which had been read out. This action yields automatic read-restore operation, i.e., any read cycle automatically becomes a read-restore cycle, greatly simplifying the memory organization and giving, in essence, the system equivalent of NDRO operation without stringent creep and threshold requirements on the film memory element. However this technique poses practical problems because of a phase difference between readout signal and required digit current.

Japanese workers[3] had considered the above technique in early dual-frequency core memories; however, it was not commonly practiced because the optimum phase angle for the digit current normally developed by the parametron was different from that of the memory readout locking signal, and a phase correction was necessary. Separate parametrons for the digit driver and the sense amplifier, coupled by buffer parametrons to absorb the phase error, were usually employed.

The use of a single word current source, switched under address control to the various word lines (as used in a linear selection memory), allows a very simple arrangement to provide the phase correction. The uncompensated phase angles of the various signals may be seen in Figure 5. Notice that the fundamental component of the readout signal is at 90° phase angle (Figure 5d) with respect to the normal buildup phase of the parametron (Figure 5a). This is in the worst possible phase for locking the parametron and minimum sensitivity would result.

The readout signal must, therefore, be shifted by 90° before it appears as a "seed" signal for the parametron. While it is possible to shift the phase of each readout signal or of each writeback digit current, a much simpler arrangement is to apply the phase correction to

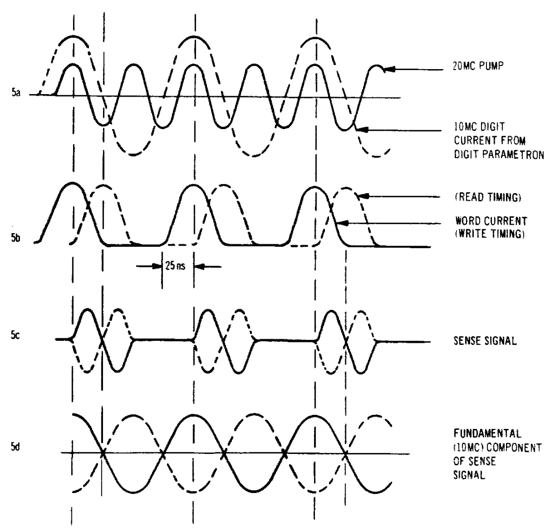

Figure 5. Timing Relations for Read-Out Phase Correction.

the word current itself. This may be accomplished by delaying the burst of unipolar pulses used for readout by the necessary amount (25 nsecs at 10 mc) to compensate for the 90° phase shift. This has the effect of shifting the sense output 90°. The burst of word pulses for the write operation is supplied without the 25 nsec delay. This is preferable to operating on the digit currents since only two word current sources are necessary; one with the correct phase for read and a second with the correct phase for write, while a phase fixup in the digit circuitry would be necessary at each digit plane in the memory.

MEMORY STACK DESIGN

Considerations of demagnetizing fields and their effect on the threshold characteristics of the memory element led to the use of a cylindrically-oriented permalloy plated wire. To produce the plated memory elements, a 10-mil beryllium-copper substrate is electroplated in a continuous process with a 10,000 Å coating of cylindrically-oriented permalloy. The H_c of the plated wire (in the cylindrical direction) is approximately two oersteds. The transverse loop shows an H_k of approximately four oersteds, with good closure of the loop to saturation.

Memory organization with a cylindrical easy direction requires that the word current generates an axial field. An efficient approach is an array of very small solenoids of the type developed previously for the Rod memory.[4] The memory stack thus consists of planes of encapsulated solenoids stacked together, with the plated wires inserted into the solenoid apertures, and connected end to end in an appropriate noise-cancelling arrangement. The plated wires themselves become the digit lines. Readout is obtained from, and digit drive is applied directly to, the plated wire lines.

The small diameter of the memory element (0.01″) requires $\approx$ 60 ma/oe for generation of a circular field (digit), which is easily provided by cylindrical thin-film parametrons.[5] The word solenoids require approximately 15 ma/oe to generate the transverse field. Figure 6 is a diagram of the stack arrangement, and Figure 7 is a photograph of a stack of 512, 26-bit words.

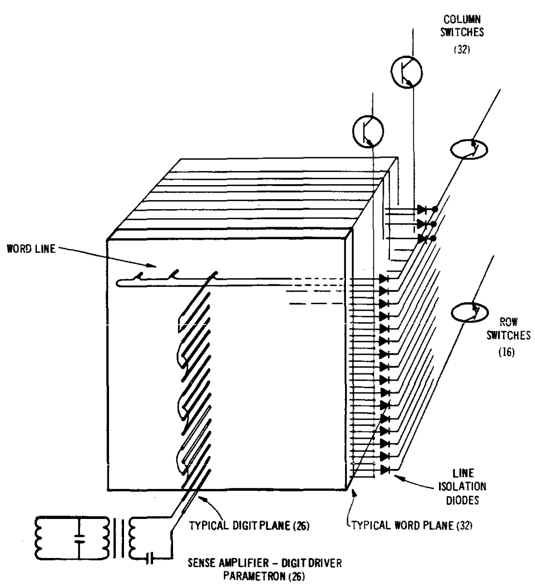

Figure 6. Stack Arrangement.

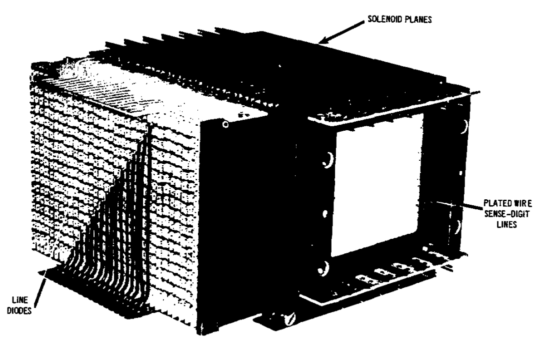

Figure 7. Phase Script Memory Stack.

The word lines are selected on a row-column basis, both ends of the lines being switched. To reduce loop inductance in the word line, a connection to the far end of the word line at the last solenoid is brought back directly under all solenoids of the same word. This places the row end of the word line close to the column end.

The sense-digit line must be treated as a transmission line, and phase errors resulting from reflections must be considered. With a conventional pulse memory, the sense line is normally terminated in its characteristic impedance. In this case the line has a resistive input impedance. An unusual advantage results from the use of parametrons as digit drivers. Since the digit current is truly sinusoidal, the line then may be treated on a single frequency basis rather than considering all spectral components of a pulse. The far end of the line may be short-circuited and a standing wave deliberately set up on the line. Since the line is short compared to the wavelength at 10 megacycles, the standing wave ratio is low (approximately 1.1:1). Thus, only a 10% difference exists between digit current in the near and far ends of the line. This has been shown to be within acceptable limits. The spatial current distribution is such that the current has the same phase angle everywhere on the line. This tolerance is perhaps more important than that of amplitude.

Since the line now has no terminating resistance to be driven, only sufficient power to overcome line losses is required. This greatly reduces (by an order of magnitude) the power necessary from the digit driver and allows the use of a simple parametron for this purpose. The inductive input impedance of the shorted line is tuned out with a capacitor, therefore a resistive load is presented to the parametron.

An interesting situation occurs when the digit line is driven in the manner described above. With reference to Figure 8, one may see that the digit current circulates in a loop, i.e., in the upper segment of the line, it circulates

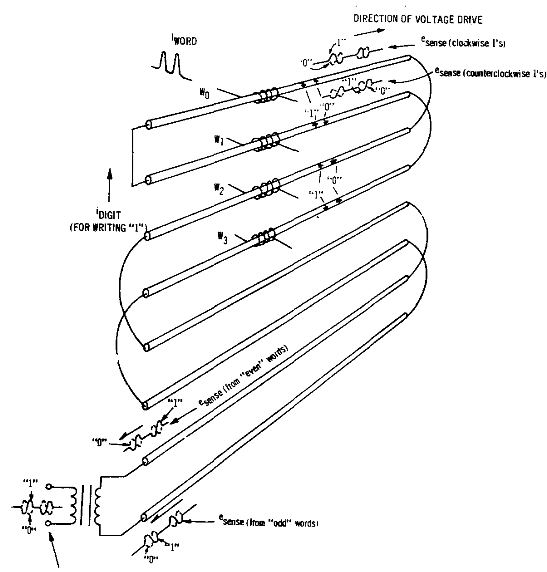

Figure 8. Digit Drive and Sense Output Polarity Relations on Sense-Digit Line.

in one direction, and in the next segment of the line, it circulates in the opposite direction. This causes opposite directions of the magnetic vector for storage of a "one" and a "zero" on adjacent pairs of plated wires. This is desirable if the input transformer for the sense-digit parametron is a differential transformer (required to reduce common mode noise). With reference to Figure 8, one sees that correct sensing of the output signal occurs and no compensation is necessary for the fact that the direction of a "one" (or "zero") alternates for "odd" and "even" words, as a result of the balanced sense-digit line.

Digit-plane to digit-plane coupling is often a source of difficulty in fast memories. A high degree of cancellation of this type of coupling is obtained in two ways: by sufficient spacing between adjacent digit planes and also by connecting the lines in such a way that the total flux induced in one line by the current in the other tends to cancel.

Four different line configurations (shown in Figure 9) are used in such a way that any pair of the four are non-interacting. By using groups of these four configurations, interaction occurs only between lines separated by four spaces, greatly reducing the effect. Each digit line, in turn, is balanced so that capacitive noise from the word lines is also cancelled by the differencing action of the parametron input transformer.

Another very unique advantage with the use of sinusoidal signals for driving and sensing is

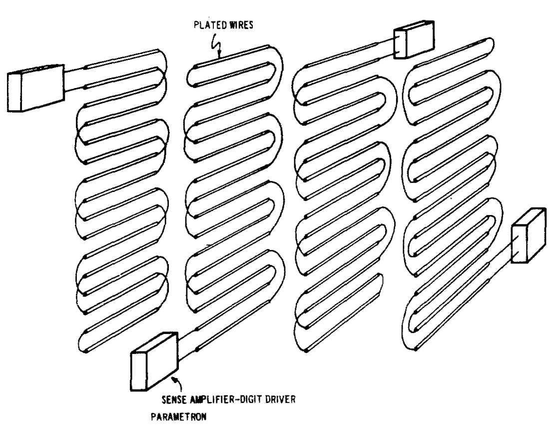

Figure 9. Non-Interacting Digit Planes.

the complete absence of pattern sensitivity for transformer coupling. A sine wave burst, the wave form of the sense signal and the digit current, may be passed through a transformer without level shift since there is no dc-base line component generated. This allows much greater freedom in the use of transformers for coupling in and out of the stack, greatly improving isolation and reducing ground noise.

MEMORY SYSTEM DESIGN

Figure 10 is a complete block diagram of the memory. In the interest of improved speed and since the actual word currents are pulses rather than sine waves, conventional row and column decoding to a matrix of saturated transistor switches is used. Diode logic is used to decode the addresses which are developed by parametron flip-flop registers driving phase-to-dc converters.

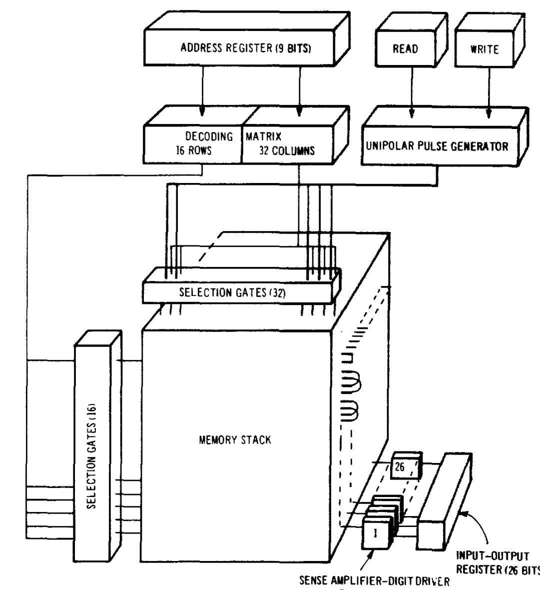

Figure 10. Block Diagram of 512 Word, 26 Bit/Word System.

Since only one word line at a time is energized, the read-write current source is simplified; the pulse current required is on the order of 100 ma at a 10 mc PRF. Figure 11 illustrates the system techniques of generating the read and write word trains with appropriate 25 nsec delay to allow optimum phase fixup for reading.

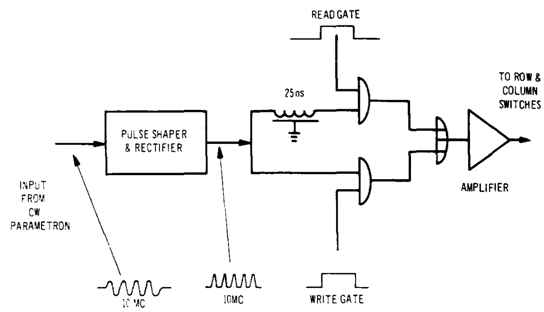

Figure 11. Word Current Shaper and Generator.

The digit parametrons are special, cylindrical thin-film parametrons, pumped at 20 mc (10 mc subharmonic) and operated in such a way as to produce approximately 100 ma pp of digit current in the line. The digit parametron also operates as a sense amplifier and is part of a three-parametron chain which forms the input-output register. Figure 12a is a schematic representation of the digit circuit.

For readout, it is necessary to insure that the sense output is the only locking signal present. This is conveniently done by cancelling the input signal from the Beat I parametron by appropriate logical gating, as shown in Figure 12b.

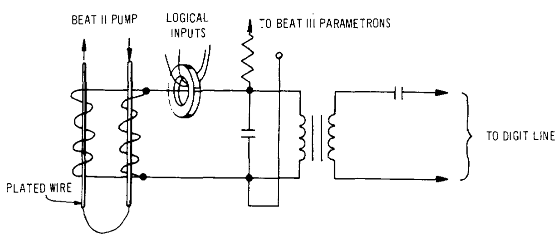

Figure 12a. Sense Amplifier-Digit Driver Parametron Schematic.

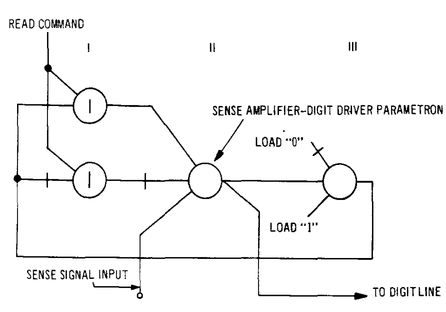

Figure 12b. Sense Amplifier-Digit Driver and Input-Output Register Logical Diagram.

If a "write only" command is to be executed, information is loaded into the register element at the appropriate time to cause the digit driver parametron (Beat II) to be at steady-state in the proper phase when the write word current is turned on.

Figure 13 is a detailed timing diagram for the memory.

The basic memory cycle is five microseconds to be compatible with the 200-kc data rate of the parametrons described in a companion paper.(5)

CONCLUSIONS

The principles of a new technique for using a thin magnetic film as a phase-script memory element have been presented. The use of cylindrically-oriented permalloy plated wire results in a simple, inexpensive memory element, with many design advantages.

Departures from previous phase-script memory techniques are the use of transverse switching with a uni-polar word pulse of the same PRF as the sinusoidal digit drive for fast writing. This eliminates the necessity for magnetic "creeping" and long write times previously encountered in other phase-script memory systems. The use of the uni-polar waveform for the word pulse eliminates the need for a word pulse PRF half that of the digit current, makes a simple row-column linear-select matrix possible, and allows generation of phase-script readout based on the fundamental harmonic component of the complex sense signal which may be used to lock a parametron operated as a sense amplifier. By a simple system artifice, an unfavorable phase relation between the readout sense signal and the required digit current may be corrected and an automatic read-restore cycle obtained by the use of a common parametron for the sense amplifier and digit driver.

The design of a 512 word (26 bits/word) memory has been described. The use of small multi-turn solenoids encapsulated in planes and assembled in arrays to form the memory stack allows reduction of word currents to moderate

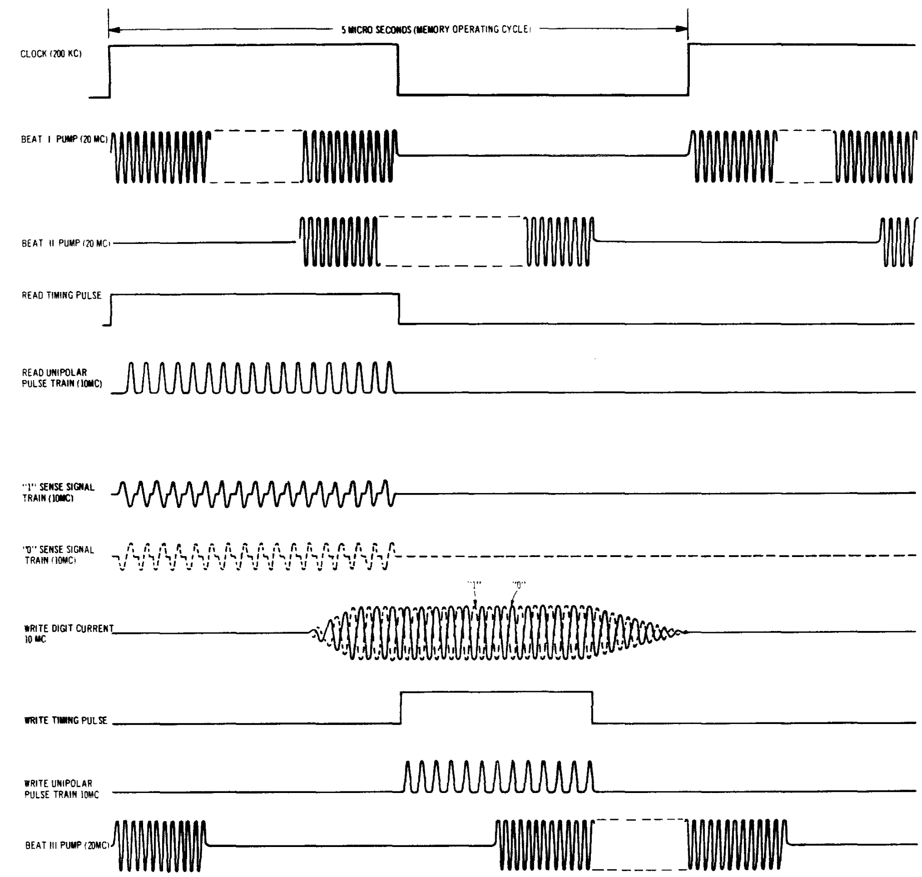

Figure 13. Memory Cycle Timing.

levels allowing simple transistor circuitry to be used. Diode logic has been used for the word decoding to achieve higher speed. It is entirely possible that an all-parametron address decoding could be utilized at the expense of speed.

Considerable sophistication has been shown necessary in the design of the sense-digit line, but the single frequency operation of this line allows many simplifications over conventional pulse memories.

It is believed that concepts leading to a low cost, moderate speed, yet highly practicable thin-film memory, that is ideally suitable for parametron computing systems, have been presented.

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