Organization and Program of the BMEWS Checkout Data Processor

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Introduction

The Ballistic Missile Early Warning System (BMEWS) Checkout Data Processor (CDP) is probably the first medium-size digital processor to perform the real-time, on-line checkout of an entire operational radar detection and processing system. This paper is the first to describe the unique organization of the BMEWS CDP and the unusual structure of its program. It also states many of the detailed characteristics of the CDP. The Checkout Data Processor has several modes of operation. As a point of reference, the mode which inserts a "realistic" sequence of events into BMEWS is focused upon in the following discussion.

The CDP has two functional memories; one for storing constants and instructions and one for storing data. The means for jointly using these two memories and still maintaining the flexibility associated with single memory machines is brought out. The features tailored in the CDP for efficiently handling its problem are emphasized. They include real-time program interrupt signals and a complex Input-Output System. This Input-Output System, as well as communicating with over a dozen other digital data handling devices, has more than 250 separate addresses.

The structure of the CDP program is the other area focused upon by this paper. The material covered describes the three separate programs which run in an interwoven fashion. This interweaving and the effect of the real-time program interrupts are brought out.

This paper is the first comprehensive public description of this major subsystem of the Ballistic Missile Early Warning System.

Role of the CDP in the BMEWS

The BMEWS Checkout Data Processor has the primary purpose of determining the operability of BMEWS by inserting either test patterns or a "realistic" sequence of events into the system, and then evaluating the BMEWS on the basis of its response.

Figure 1 illustrates the way the CDP fits into the BMEWS. In the normal or real situation, a radar data take-off collects radar returns on a target and assembles these to produce a report. Each report is transferred to the missile impact predictor which stores and correlates the various radar data take-off reports. On the basis of these reports, the missile impact predictor prepares various reports such as a report containing the values of the parameters associated with an observed missile trajectory.

The CDP controls the insertion of a simulated sequence of returns into the front end of BMEWS. At the same time, the test tag is issued to the appropriate radar data take-off to indicate that the return is simulated. The test tag remains with the data throughout the system to differentiate test information from real information. As the radar data take-off correlates the simulated returns, the report that is produced and sent to the missile impact predictor, is also sent to the CDP.

The missile impact predictor uses the data take-off reports to produce reports of its own. These reports are also sent to the CDP.

Organization of the CDP

It is convenient to consider the CDP as being composed of five major subsystems; Wired-Core Memory, Coincident-Current Memory, Arithmetic and Logic Unit, Input-Output System, and Control System. A block diagram of the CDP subsystems and their interrelation is illustrated in figure 2.

Wired-Core Memory

The Wired-Core Memory, which is a form of the Diadem ring translator, stores the program and constants used by the CDP. It contains 4,096 storage locations. A Wired-Core Memory was chosen for two reasons; namely, speed and reliability. Figure 3 illustrates the instruction word format as it appears in Wired-Core Memory. Since the CDP has two diverse types of memories, the locations of each of the types of memory are called by different names. The Wired-Core Memory locations are called "locations" and the Coincident-Current Memory and input-output locations are referred to as "addresses".

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Bits X₀, X₁, and X₂ are used to specify the operation modification. Four configurations of X₀, X₁, and X₂ are interpreted as follows: when X₀ is zero the operation is specified by X₃ through X₇ with X₈ through X₁₉ specifying the accompanying address or location. Bit X₂ is the parity bit associated with X₃ to X₇. Three other configurations of X₀, X₁, and X₂ when X₀ is one specify an operation to be performed with a constant. In these cases X₄ to X₁₉ are used to specify the constant. These bits are actually transferred into the arithmetic unit as data.

In the normal operations, i.e., when the operation modifier indicates that X₃ through X₇ is to be interpreted as the operation and not part of a constant, X₂₀ through X₂₂ are used to indicate which of the index registers are to be used with the instruction. There are three independently used index registers. There is one exception to the above statement in which X₂₀ through X₂₂ indicates a specific bit in the accumulator which is to be tested.

One of the tailored features of the CDP is concerned with performing table lookups of constants stored in the Wired-Core Memory. The sequence of instructions is initiated by a normal instruction which performs two functions. The first function is to store the location of the next instruction in a fixed address of the Coincident-Current Memory. The second function is to jump to the address specified in the instruction itself. This address may be modified by the various index registers. The jump leads to an instruction which contains an operation modification. This operation modification adds the constant specified in the instruction into the arithmetic unit and then control is transferred to the location specified by the fixed address in Coincident-Current Memory. This same technique can also be used to enter and leave sub-routines as well as perform table lookups.

Another feature added to the instruction repertoire to give desired flexibility in using the Wired-Core Memory is an indirect jump. This instruction, in Wired-Core Memory, specifies an address in the Coincident-Current Memory which contains the location in the Wired-Core Memory to which control should be transferred. Thus, variable linking can be accomplished by changing the contents of the Coincident-Current Memory address involved.

### Arithmetic and Logic Unit

The Arithmetic and Logic Unit contains an accumulator and associated registers and control circuits for carrying out addition, multiplication, subtraction, division, shifting, masking, and so forth. This unit obtains input data by directly addressing the Input System or via the Coincident-Current Memory. The Arithmetic and Logic Unit also directly sends information to the Output System. The data derived from the addressable inputs or sent to the addressable outputs are used in essentially the same way as data sent to and from the Coincident-Current Memory. For example, one input address contains the azimuth position of one of the radars. The contents of this address can be read into the accumulator as though it were data from the Coincident-Current Memory.

### Coincident-Current Memory

The Coincident-Current Memory of the CDP is composed of 1,024 addresses. This memory has several functions. One of these functions is to act as an input buffer for various real-time asynchronous input sources. There are buffers for data reports from the radar data take-offs and reports from the missile impact predictor as well as information from an input magnetic tape. Also, there is an output buffer which is used to store information required in simulating RF returns. When a data word is required by or available from an outside source, the program is interrupted for a memory cycle during which time this data word is removed from or stored in an allocated address in the Coincident-Current Memory. The interruption occurs without the knowledge of the program.

Other functions of the Coincident-Current Memory include storing intermediate results and control information developed and used within the program. Also, the indirect address feature and standard address feature previously mentioned are facilitated by the use of Coincident-Current Memory.

### Input System

The Input System can be considered as composed of two diverse parts. There are demand inputs which supply information such as the radar position vector and console commands, and asynchronous inputs which supply magnetic tape information and system reports. Each separate demand input is associated with a particular address. As was stated previously, these addresses can be read or acted upon in a normal fashion. There are over 180 addressable inputs which fall into 36 different classes of information. The Input System has the facility for communicating with well over a dozen other digital data handling devices including a pair of IBM 7090's.

The asynchronous inputs are stored in the Coincident-Current Memory by interrupting the program control over the memory for single read-write cycles. Beside information from the input magnetic tape, the CDP receives, by means of this Coincident-Current Memory...
interrupt feature, 12 different types of messages from other processors in the system with an average of six to seven items per message type.

**Output System**

The Output System has the same dichotomy as the Input System. There are over 75 addressable outputs which fall into about 15 classes. A major portion of the Output System is associated with a target simulator which actually produces the simulated returns and accompanying test tags. Figure 4 shows one of the target generators of the target simulator. An output address is associated with a digital-to-analog converter (DACON) which is used to control the amplitude of the desired output signal. Another DACON, which is loaded by the program, controls a variable frequency oscillator (VFO). The modulator controls the amplitude of the output signals generated by the VFO. The range value is placed into a counter by the program at some time prior to the initiation of the radar main bang. At the beginning (leading edge) of the main bang, an oscillator is connected to this counter providing an output at an appropriate time to simulate a return at the range desired. This counter output lasts for the duration of the desired return. As a result, the output of the target generator is a pulse of the correct amplitude and frequency at the desired time to simulate the return from a target at the corresponding range. It is worth noting at this point that the CDP acts as the controlling element in a feedback loop for the variable frequency oscillator. The output of the VFO is fed into a counter for a fixed period of time. This average frequency is sampled by the program to produce a new value to obtain the desired frequency. The new value is placed into the digital to analog converter which controls the VFO. This subject will be discussed in a later paragraph.

A summarizing fact which further indicates the unusual complexity of the Input-Output System is that there are more than 1,300 connections for the addressable inputs and outputs alone.

**Control Unit**

The Control Unit, besides containing the facilities usually associated with control functions of internally stored program digital computers, has five features used in interesting ways. The first of these features, which was mentioned previously, is the ability to recognize signals from the Input-Output System. These signals indicate to the Control Unit that a memory cycle is to be usurped for asynchronous input-output reasons. The Control Unit has a built-in priority system to handle simultaneous input-output requests as well as the address control for storing the data.

Another feature, also previously mentioned, is the incorporation of a timer in the Control Unit to establish the sampling period for measuring the variable frequency oscillator outputs. This is a two-phase timer that allows the sampling of the VFO output to take place for a fixed period of time followed by a period of time during which no sampling takes place. This dead period is used by the program to compute the necessary corrections and also to apply new inputs to the VFO's.

One of the more highly tailored features of the CDP is the three index registers and their use. The discussion of these index registers is included in the Detailed Characteristics Section. Other features associated with the Control Unit are the inclusion of a special tag register and the presence of program interrupt signals which relate to the occurrence of the radar main bang. These features are discussed in the Programming Section.

**Detailed Characteristics**

A binary numbering system is used in the BMWS CDP with a data word length of 18 bits plus one bit for parity. Accessing an instruction from the Wired-Core Memory and modifying the address by index registers requires four microseconds. There are two memory accesses per instruction: one memory access of the Wired-Core Memory for the instruction itself and another access from the Coincident-Current Memory or input-output address. In either case, 8.8 microseconds is involved in the access and manipulation of data for basic instructions. Therefore, an instruction such as an addition requires 12.8 microseconds to complete; including the instruction access and modification of the address by index registers.

The CDP uses 27 out of the 32 possible instructions facilitated by the five bits of the operation code. There are also the three operation modifications for use with constants.

The Wired-Core Memory contains 4,096 - 23-bit words. The Coincident-Current Memory contains 1,024 - 19-bit words. Both memories use a binary addressing system and all data and instructions are addressable by words.

The CDP contains three index registers - a three-bit register, a four-bit register and a five-bit register. The contents of each of these registers are logically added to the address contained within the instruction.

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1. Reference to a radar main bang is confined to the leading edge. Reference to an inter-pulse period is defined as the time between successive main bangs.
There is no time penalty associated with the use of the index registers. The index registers mix into an address in the following fashion:

\[
\begin{align*}
3 \text{ Bit Reg.} & \quad 5 \text{ Bit Reg.} \\
X_8 & \quad X_{10} X_{11} X_{12} X_{13} X_{14} X_{16} X_{17} X_{18} X_{19} \\
4 \text{ Bit Reg.}
\end{align*}
\]

There are specific operations which use indirect addressing only. There is no time penalty associated with such operations, that is, they require 12.8 microseconds to carry out.

The BMEWS CDP is capable of simultaneously carrying out input operations while performing arithmetic computations. For example, the program performs a single instruction which is a start-tape command. The program then ignores the tape input operation, while performing arithmetic operations, until an appropriate time when an inspection of the tape input buffer reveals the required information.

Information is stored on the input magnetic tape as 6-bit characters plus a parity bit (character parity is odd). There are 120 characters to a tape record. Three 6-bit characters are assembled by the Input System to form one 18-bit CDP word. Thus, the input magnetic tape buffer size (in Coincident-Current Memory) is 40-CDP words. The Input System supplies an entire word to Coincident-Current Memory during each transfer operation. The nominal tape reading speed is 15,000 characters per second.

The output console printer is controlled by a 40-bit buffer which is addressable by the CDP. These 40-bits are composed of ten 4-bit characters. The printer operates at twenty 10-character lines per second.

The clock rate of the CDP is 1.25 megacycles. It contains about 8,000 transistors and between 40,000 and 50,000 diodes. The CDP is mechanized by NOR type transistor-diode logic.

**Structure of the CDP Program**

The CDP program must carry out the functions associated with several checkout modes. Each of the modes is designed to evaluate the BMEWS from a slightly different point-of-view. Some modes insert "realistic" raids into the BMEWS while other modes insert test patterns into the BMEWS. The CDP program is composed of three parts; the simulation program, the evaluation program, and the executive program. These programs are used in all of the checkout modes.

Each of the programs is composed of routines. The mode determines which routines of each program are to be used for the processing.
simulation program are of such nature that they must be completed by specified times in order to be of use. Therefore, these routines are synchronized by the program interrupt signals.

The simulation program performs three major functions. These are:

1. Determines the system status (connections between BMWS major sub-systems).
2. Controls the target simulator.
3. Prepares the values for the parameters of anticipated messages for use by the evaluation program.

The evaluation program processes the information received by the CDP from the BMWS in order to evaluate the operability of BMWS. There are also evaluation routines used to organize information to be printed out; this information is pertinent to the evaluation of the operability of BMWS. Likewise, there is a routine in the evaluation program for determining CDP failures. Evaluation routines, unlike the simulation routines, do not have to be kept in step with events of each main bang period, but must only meet time requirements in the large. The evaluation program, once started, continues from evaluation routine to evaluation routine until interrupted by a program interrupt signal.

The evaluation program is divided into three priority classes of routines; routines corresponding to a given mode of operation of the first class precede those of the second class which in turn precede those of the third class within a main bang period. The highest priority classes are always initiated in each main bang period (or continued if it has been interrupted, see below). This highest priority class is initiated by the executive program after program interrupt 1 (see figure 6). The three sets of evaluation routines are called Class I, Class II, and Class III with the highest priority being Class I, the next priority Class II, and the lowest priority Class III. Thus, the uninterrupted processing sequence would have the Class I routines processing all their applicable data, followed by the Class II routines processing all their applicable data followed by the Class III routine. The Class III routine (error detection routine) is a non-ending routine, i.e., the "end" of the routine leads back to the beginning.

The CDP program is organized to begin the processing of a given class of evaluation routines at the point of interruption of the interrupted routine of that class. If a given evaluation process was not interrupted then processing begins at the first routine of that class.

Figure 5 illustrates the organization of the three classes of the evaluation routines in the CDP program. The possible returns to the evaluation program are shown inside the executive program. Note that there is a path from each interrupt to the starting of the Class I routines each main bang.

The evaluation program performs three major functions. They are:

1. Process messages received from the rest of BMWS - using anticipated values from the simulation program.
2. On the basis of (1) - turn on appropriate console lamps and printout appropriate information.
3. Check the operation of the CDP itself.

The evaluation of system reports is illustrated in figure 7. The evaluation routine picks up the value for each of the parameters in the received report and subtracts the corresponding anticipated value. A new message is composed which contains the message type, the target tag, the anticipated value for each of the parameters and the calculated difference between the received value and this anticipated value. This new message is a candidate for printout. The criterion for printing the message is that the deviation of the value for at least one of the parameters is larger than the specified tolerance. If all of the deviations are within the specified bounds, normally, the message is discarded. However, subject to a switch setting on the console, all such printout candidates can be printed out for the purpose of data collection. An out of tolerance deviation is marked appropriately to identify this situation to the operator.

Summary

A program interrupt occurs at the beginning of the radar main bang (figure 8). This interrupt causes the executive program to store the state of the CDP and proceed into the simulation program. The simulation routines, which are carried out at this time, control the variable frequency oscillators of the target simulator and check to see that the BMWS status has remained stable. That is, there has been no change in the way the major subsystems of BMWS have been linked together. The completion of these two routines returns the program to the evaluation program by way of the executive program.

The evaluation program inspects the Coincident-Current Memory for information coming into the area reserved as system report input buffers and, if information has
been received, compares these reports with anticipated reports also stored in the Coincident-Current Memory by the simulation program. The evaluation program is eventually interrupted by program interrupt 1. Console switches are inspected to see that the CDP is still to remain in the present mode or change modes. The simulation program is then initiated.

The simulation routine which is carried out at this time calculates the inputs required by the target simulator at the end of this main bang to simulate returns following the subsequent main bang. This calculation is based upon the system status, the particular position of the various beams, and target data which had previously been stored in the Coincident-Current Memory by the magnetic tape portion of the Input System. The simulation routine, prior to starting its calculation, initiates the reading of a record from the input magnetic tape for use during the next inter-pulse period. Data used in this inter-pulse period had been read in during the previous inter-pulse period. The results of the calculation of this simulation routine are stored in Coincident-Current Memory ready for transfer to the target simulator at an appropriate time.

The evaluation program is then re-entered via the executive program. Here the executive program restarts the Class I routines if they had not just been interrupted. If they had just been interrupted by program interrupt 1, the interrupted situation is resumed. Again the evaluation program continues until the next program interrupt occurs. At this point, the executive program leads to the simulation routine that transfers the information previously calculated for the target simulator into the target simulator.

The target simulator must be quiescent during the period of time that the program transfers new parameter values into the range counter. Therefore, the maximum range that can be simulated is limited by the period of time associated with this transfer. In actuality, program interrupt 2 marks the end of time when the target simulator is capable of producing a simulated return during the main bang.

Thus, each main bang, data taken from the input magnetic tape during the previous main bang and stored in Coincident-Current Memory is used together with system information to produce control information for the target simulator. This information is transferred into the target simulator at the end of the main bang. During the next main bang, while this same calculation process is being repeated, the target simulator inserts into the system, if required, simulated RF returns and corresponding test tags. This process continues main bang interval after main bang interval.

The radar data take off correlates the inserted signals and issues reports to the missile impact predictor. These same reports are shipped to the CDP and stored in the appropriate area of the Coincident-Current Memory. The evaluation program continues to inspect this portion of the Coincident-Current Memory sensing for such reports. When a report is received, it is evaluated by using the anticipated report produced by the simulation program. If an out of tolerance situation is discovered, information is shipped out to the operator by means of the printer.

Radar data take off reports are collected by the missile impact predictor and used to produce various other reports. These reports are shipped to the CDP and stored in the Coincident-Current Memory. In a similar fashion, the Checkout Data Processor compares these reports with anticipated reports and indicates to the operator the result of such processing. In this way, the Checkout Data Processor using its equipment and its program in an interwoven fashion, generates simulated RF returns, injects these returns into the front end of BMWS, receives the effect that these signals have on BMWS, and on the basis of these effects, evaluates the operability of the overall system. Finally, the checkout device, being a major part of BMWS, evaluates its own operability.
Figure 1. CDP in the BMEWS
Figure 2. Organization of the CDP
Figure 3. Wired Core Memory Word Format
Figure 4. Target Generator
Figure 5. Organization of the CDP Program
Figure 6. CDP Program Timing
Figure 7. Evaluation Process