The System Organization of MOBIDIC B

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MOBIDIC B is an all transistorized, militarized computer mounted in a standard Army trailer. It is a general-purpose, parallel, binary, synchronous, fixed point, and duplexed data processing system.

It contains two basic processors, identical in characteristics and internally tied to the same system transfer bus. Both processors share a common set of input-output devices and each processor is capable of operating on an independent program without interference. They are also capable of duplex operations, allowing either processor to monitor and exert control over the other.

In addition to the 8192-word high speed Core Memory in each processor, there exists a 50 million-bit Mass Memory. This memory is treated as an input-output device, addressable by in-out instructions. A Data Retrieval Unit is incorporated to facilitate data searching from the Magnetic Tape and the Mass Memory. The control console is also duplexed, containing two independent and identical panels, one for each processor.

Introduction

There are a number of large-scale, general-purpose, mobile digital computers being developed at Sylvania[1]. They are known as the MOBIDIC family of computers. MOBIDIC C and D are identical in internal design to MOBIDIC A[2]. They differ only in peripheral equipment.

MOBIDIC B is the second member in the MOBIDIC family. It will be used primarily in the field to meet the Army's data processing requirements, and is to be installed in a standard 30 foot Army trailer. MOBIDIC B contains all the instructions utilized in MOBIDIC A and also an additional 12 new instructions. To minimize equipment, some of the instructions have been made subroutines which are initiated automatically.

MOBIDIC B is a duplexed data processing system. It contains two identical central processors connected to a common system transfer bus. Each central processor has an individual real time system which provides direct communication with external FIELDATA equipment. Each of the two central processors is a general-purpose computer. They can use any of the input-output devices available and either processor can run separate programs without interference from the other. In addition, the two processors can operate together and communicate with each other through an in-out device such as a magnetic tape. Either processor can use the other's core memory through an input-output device. It is also possible for either processor to monitor and exert control on the other through the direct connections between them.

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[1] J. Terzian, "MOBIDIC Computer Series," THE SYLVANIA TECHNOLOGIST, Vol. XII, No. 3, July, 1959, pp. 58-64.

[2] J. Tersian, "System Organization of MOBIDIC A," presented at the 1957 WESCON Convention, August 20, 1957, San Francisco, California.

Special Requirements

There are 4 major requirements of a special nature imposed on this computer. The first is that MOBIDIC B is to be a duplexed data processing system. The second requirement is that it must be compatible with other MOBIDIC computers. Compatibility is sought not only through instruction type and word format, but also through the interchange ability of input-output devices and the physical element-cards and packages. Minimum equipment is another design criterion. This is achieved by having all full-length registers simulated in the core memory and also by mechanizing some of the infrequently used instructions through automatic subroutines. Only two full-length working registers are used within each processor. Data retrieval capability is the fourth of the special requirements. Data stored on either the magnetic tape or the mass memory must be retrieved at full device speed. This continuous and speedy retrieval ability necessitated the incorporation of a data retrieval unit together with the addition of some special instructions.

Instructions and Word Format

Instructions

There are 64 instructions in MOBIDIC B (Table 1). They are classified into 3 categories, namely, directly-mechanized instructions, subroutine instructions, and special instructions. There are a total of 40 directly mechanized instructions. In most cases, the execution time has a variation of 2 μs. The instruction LGM, for example, may sometimes be executed in 36 μs instead of the 38 μs shown in Table 1. The variation is due to the fact that the system bus is time-shared by both processors. The system bus may or may not be available to the processor which is executing the instruction that requires access to it at that particular instant. The times given in Table 1

TABLE I

MOBIDIC B INSTRUCTION REPERTOIRE

Op Code	Abbr.	Time (μs)	Type			Instr. Description
			Direct	Sub	Special	
00	HLT	24	D			Halt
01	RPT	—		R		Repeat
02	LGM	38	D			Logical multiply
03	LGA	38	D			Logical add
04	LGN	36	D			Logical negation
05	SEN	28	D			Sense
06	SNS	28	D			Sense and set
07	SNR	28	D			Sense and reset
10	CLA	36	D			Clear and add
11	CAM	36	D			Clear and add magnitude
12	ADD	44	D			Add
13	ADM	44	D			Add magnitude
14	CLS	36	D			Clear and subtract
15	CSM	36	D			Clear and subtract magnitude
16	SUB	44	D			Subtract
17	SMB	44	D			Subtract magnitude
20	MLY	88–774	D			Multiply
21	MLR	88–786	D			Multiply and round
22	DVD	—		R		Divide
23	DVL	—		R		Divide long
24	ADB	—		R		Add beta
25	SBB	—		R		Subtract beta
26	BSPL	—			S	MOBIDIC B special
27	BSPL	—			S	MOBIDIC B special
30	SHL	30–66	D			Shift left
31	SLL	46–118	D			Shift left long
32	SHR	30–66	D			Shift right
33	SRL	—		R		Shift right long
34	CYS	30–66	D			Cycle short
35	CYL	—		R		Cycle long
36	SLA	30–66	D			Shift left and logical add
37	NRM	—		R		Normalize
40	TRU	28	D			Transfer unconditional
41	TRL	—		R		Transfer & load PCS
42	TRS	—		R		Transfer to PCS
43	TRX	—		R		Transfer on index
44	TRP	26	D			Transfer on positive
45	TRZ	26	D			Transfer on zero
46	TRN	26	D			Transfer on negative
47	TRC	—		R		Compare
50	STR	34	D			Store
51	LOD	36	D			Load
52	MOV	36	D			Move
53	LDX	—		R		Load index
54	RPA	—		R		Replace address
55	MSK	—		R		Mask
56	BSPL	—			S	MOBIDIC B special
57	TRY	38	D			Transfer on index B
60	BSPL	—			S	MOBIDIC B special
61	BSPL	—			S	MOBIDIC B special
62	BSPL	—			S	MOBIDIC B special
63	BSPL	—			S	MOBIDIC B special
64	BSPL	—			S	MOBIDIC B special
65	BSPL	—			S	MOBIDIC B special
66	SKP	30	D			Skip
67	BSP	30	D			Back space
70	RAN	30	D			Read alphanumeric
71	RRV	30	D			Read reverse
72	ROK	30	D			Read octal
73	SCH	30	D			Search
74	WAN	30	D			Write alphanumeric
75	WWA	30	D			Rewrite alphanumeric
76	WOK	30	D			Write octal
77	RWD	30	D			Rewind

are maximum.

There are 15 subroutine instructions. These instructions are performed through subroutine programs, which must be stored in memory and executed automatically. As such, all instructions used in the program to execute the sub-routine instruction must be of the mechanized type. Nine of the MOBIDIC B OP codes are unassigned. They are available to perform any special subroutine operation that may be required in a particular application. Whenever one of these "special" instructions is decoded, operation is automatically transferred to a unique location from which the program is re-routed to the desired subroutines.

According to their logical functions, the 64 instructions can be classified as follows: 16 arithmetic operations, 17 sequencing and indexing, 10 input-output; 12 editing and data handling; and 9 special purpose instructions.

Word-Format

The length of the MOBIDIC B word is 38 bits, the length used in other MOBIDIC computers. The word format is illustrated in Fig. 1. Numerical data is represented by a fixed point, magnitude and sign conventions. Magnitude is registered in bits 1 to 36. The binary point is understood to be placed between bits 36 and 37. Bit 37 is used for sign of a number stored and bit 38 is used as a parity check bit. Alphanumeric data is represented in the same manner as numeric data, except that the sign bit is eliminated and the 36 bits are grouped into 6 alphanumeric characters. Since MOBIDIC uses a weighted code, alphanumeric data can be sorted without conversion to binary form by direct use of the logical and arithmetic operations.

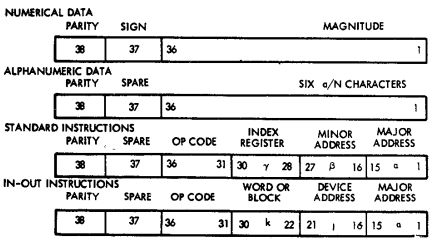

Fig. 1—MOBIDIC B word format.

A standard instruction word is divided into 6 parts:

(1) Major Address (α): Bits 1 to 12 specify a memory address while bits 13 to 15 specify which memory will be used. Since many of the internal MOBIDIC B registers are addressable, one of the eight configurations for bits 13 to 15 represents internal register addresses. The actual register addresses in these cases are specified by bits 1 to 5.

(2) Minor Address (β): Bits 16 through 27, the β bits, have several uses, depending on the particular instruction being performed. They may be loaded into or added to the contents of an index register. The β bits, either alone

or in combination with γ may also be used to specify a second address.

(3) Index Register (γ): Bits 28 to 30, γ bits, are used primarily for indexing. They specify which, if any, of the Index Registers are to be used with the instruction. For some instructions, γ is used as part of a second address.

(4) OP Code: Bits 31 to 36 designate the instruction to be performed.

(5) Spare: Bit 37 is a spare.

(6) Parity: Bit 38 is the parity bit.

The format for input-output instructions is identical to that of standard instructions except for the assignments made to bits 16 to 30, the j and k portions of an in-out instruction. The j bits, 16 to 21, are used to specify the particular input-out device addressed. Sixty-three input-output devices may be handled in this manner. The k bits, 22 to 30, are used to specify the number of words or blocks to be processed.

Overall System Description

The block diagram of the MOBIDIC B system is given in Fig. 2. In it are shown: two identical computers (processor 1 and processor 2), two in-out converters, a data retrieval unit, a mass memory unit, two real time systems, and a family of in-out devices. The two processors are fed by a common system clock to facilitate system synchronization. They are connected to a comon system transfer bus and also share the same in-out system. The processors can operate independently as separate computers or can communicate with each other through magnetic tape. It is possible for either of the two processors to give a set of instructions which will read from or write into the memory of the other processor. It is also possible for one processor to monitor the other through the signal lines connecting them directly. Furthermore it is possible for one processor to control and give commands to the other processor.

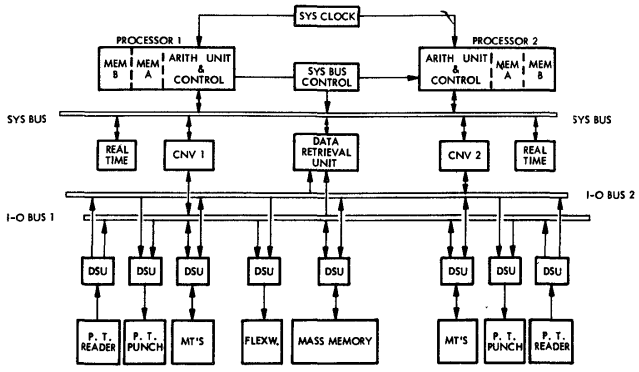

Fig. 2—MOBIDIC B system block diagram.

The converters serve as format control and synchronizing buffers. They are capable of handling all devices including the mass memory unit. The converters are assigned to either of the two processors on a first-come-first-serve basis. Since the two processors are connected to a common system bus, it is entirely possible that both may want to get on the system bus at the same instant. To avert this uncertainty, the system bus control circuit is used to continuously assign the system bus to the processors alternately. Each is given a 2 μs period to use it. Therefore, a waiting period of 2 μs may be required at an arbitrary time. The danger of both processors trying to get to the same converter is also avoided by the same control circuit.

In addition to the standard family of MOBIDIC in-out devices, the MOBIDIC B system includes a 50-million-bit memory which is also treated as an in-out device. Data transfer to and from the mass memory will be handled by the converter through the in-out bus. The data in the mass memory is arranged in blocks, separated by block start and block end marks. The block number on each track is addressable. Both the track and block addresses must be loaded into the mass memory control unit prior to giving the write or read instruction. These addresses are sent out from the processor through the converter, similar to the manner by which the data is transferred.

The data retrieval unit is designed to assist the open format search program. A retrieval program examines the specified fields to determine whether or not the search criteria are satisfied. Closed format search can be accomplished entirely by programming and does not require any auxiliary equipment.

The two real time systems enable the processors to communicate with other data processing equipment external to the MOBIDIC B system. Each has a fixed assignment to serve one definite processor and is not accessible to the other processor.

On the other hand, the balance of the entire input-output system does not have a fixed assignment. Operating on a first-come-first-serve basis, it is entirely possible for one processor to automatically monopolize the use of both converters, the data retrieval unit and a complement of devices. Without a converter the other processor cannot reach any device even if it is available. Under such a circumstance, the other processor would have no choice but to wait for a converter to become available. In some special cases, the other processor may have just received, through its own real time system, an urgent request which requires data processing through the service of a converter. Upon receiving such a request, it is possible for the other processor to shorten the in-out operation of the first processor, making the converters available.

Brief Description of Processor

Since minimum equipment is a major design re-

quirement, most full length registers normally existing in other MOBIDIC Computers are stored as locations in the memory. These reserved memory locations are referred to as simulated registers. Simulated registers include the accumulator, the Q-register, the B-register, the program counter, the program counter store, and seven index registers. They can be addressed in exactly the same way as their counterparts in other MOBIDIC computers. As shown in Fig. 3, only two full-length physical registers are used in each MOBIDIC B processor, the memory register (MR) and the control Register (CR). These registers and other essential parts in the processor are described as follows:

Timer The timer, containing three counters, receives pulses from the system clock. The processor executes instructions by proceeding through a sequence of events. Certain events, such as memory operations, occur so frequently that a separate counter TM is used to control these operations. The execution of instructions requires several memory operations. Counter TI indicates which of the several memory operations is currently in progress. Finally, if an input-output access to the central processor is required, the instruction execution must be interrupted and a new sequence of events must start. A third counter TB controls these input-output processing operations.

Core Money Each processor of the MOBIDIC B system is provided with two 4096-word core memories with a read-write cycle of 8 μs. It can be readily expanded to 4 memories per processor when desired. It can be ultimately expanded to 7 memories, totaling 28,384 words.

Memory Register The MR is directly connected to the memory. It is a 38-bit register and is used as the memory in-out register. The MR is also used as an arithmetic register during execution of the instructions.

Control Register The CR serves primarily as a 37-bit arithmetic register corresponding to the accumulator in MOBIDIC. In addition, the first 15 bits of CR are also used as the memory address register during initial access to the high-speed memory.

Decoder Register This is a 6-bit register used to store the instruction while it is being executed. Its output interprets the instruction stored and energizes appropriate control lines to initiate execution of the instruction specified.

Control The control unit contains the logical circuits to control all of the detailed operations of the computer.

Special Address Control The special address control unit contains the decoders and control circuits to address the core memory locations which are reserved for special registers of the processor and the data retrieval unit. Among the registers specified by the special address control unit are most of the simulated registers. The contents of these registers can be transferred to the MR and then to the CR whenever it is requested.

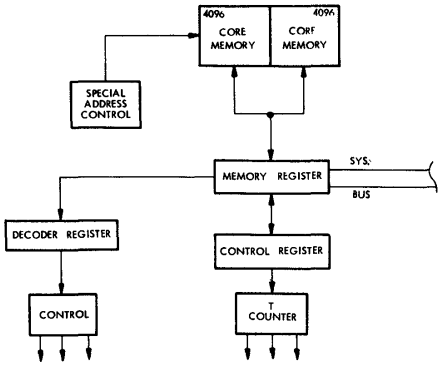

Fig. 3—MOBIDIC B processor.

T Counter The T Counter is a 7-stage counter used in both shifting and multiplying operations.

System Clock The system clock provides standard p and t pulses spaced one microsecond apart to the entire system. There is a separate clock for each processor. This makes the processors identical. One system clock may be used to control the entire system operation when the processors are working together, depending upon which processor is in full control of the program.

System Bus Control The system bus control circuits regulate and direct the flow of traffic between the two in-out converters, the data retrieval unit, and the two processors. These control circuits give either processor access to the system bus.

Input-Output System

A more detailed description of the various components in the In-Out system will now be given. Reference should be made to Fig. 2.

In-Out Converter There are two in-out converters in MOBIDIC B. They are used as buffers between the input-output devices and the central processors. They assemble data coming in from a device and put it into MOBIDIC word format before transferring it to the central processor. Conversely when data is to be sent out to the device from the central processor, the converters decompose the standard MOBIDIC word and reassemble it into the proper format for the particular device which is to receive it. In addition, converters also have the function of synchronizing the operation of the devices with that of the central processor. In this way, the information transfer between the converter and the device can take place quite independently from the operation of the central processor. Internal computation is only interrupted during access to the memory.

Data transfers between converters and processor

memories are handled on a "busy-bit" basis over the system bus. As soon as a converter is selected the processor will transfer the entire in-out instruction to the converter. The processor subsequently goes on to execute the next instruction and exerts no further control over the converter. The converter, taking upon itself to execute the instruction it has just received, proceeds to communicate with the device addressed and sends out or receives data from the device. When the converter is ready to send in or to receive another word from the processor, it will signal the processor by raising a busy-bit. Detecting a busy-bit, the processor will interrupt its operation and take care of the converter.

Real-Time System There are two identical real time systems. Each system consists of an input register, an output register and an input address register. Each real time system is assigned to a processor. These real time systems can be used to provide the communication link between the two central processors of a single MOBIDIC B system, between two MOBIDIC B systems, between a MOBIDIC B and MOBIDIC A computer or with other FIELDATA computers and communication equipment. In all cases except the last, the real time output register in one real time system can be directly connected to the real time input register of the other real time system. In the FIELDATA application, a buffer unit may be required between the real time system and the external equipment. For example, a Kineplex is required when the teletype communication equipment is connected to MOBIDIC B.

Data Retrieval Unit The DRU is a special unit designed to assist the data retrieval program from the storage fiiles. It is connected to the system bus as well as the in-out bus. It will examine all the data being transferred from the magnetic tape (or mass memory) to the converter. After extracting the desired portion, the data is then sent to the core memory for further processing.

Mass Memory The mass memory is needed to provide an exceptionally large data storage capability. It consists of 8 magnetically coated discs, giving a total of 16 usable disc sides. There are 4,096 tracks on which the data can be stored. Storing is done in a serial-serial manner which can be continuous from one track to the next. Track switching is done automatically. There are two magnetically engraved clock tracks, one at 150 KC bit rate and the other at 225 KC bit rate. The maximum random access time of the mass memory is less than 0.25 seconds.

Magnetic Tapes A total of 8 magnetic tapes are currently provided in MOBIDIC B. They could be either the commercial FR-300 type or the militarized type. They have 8 channels which incorporate a parity error detection channel. The nominal tape speed is 150 inches per second (reversible) with approximate start and stop time of 1.5 ms. The nominal character rate is 45 KC.

Flexowriter The Flexowriter is a special electric typewriter that operates at a speed of 10 characters per second. It can be used on- or off-line or as an output device for producing hard copy or punched paper tape.

Paper Tape Reader There are two photoelectric paper tape readers, one being a 5-hole and the other an 8-hole reader. These input devices have a nominal reading rate of 270 characters per second.

Paper Tape Punch The two paper tape punches include a 5-hole punch and an 8-hole punch; both are directly adaptable to the reader. Both types prepare punched paper tape at a nominal character rate of 100 per second.

Duplexing Capabilities

The two MOBIDIC B processors are tied to a common system bus and share a common set of in-out equipment. It is beyond the scope of this paper to give a detailed description of the entire duplexing capabilities existing in MOBIDIC B. A separate technical paper is to be published treating this subject in greater detail. Briefly, there exists a set of control lines connecting the two processors directly. Through these lines the operating status of one processor can be monitored by the other processor. Through these control lines also, one processor can exert control and give command to the other processor in a limited manner. In particular, one processor can prevent the other from coming to a complete halt condition, thus keeping the other processor in a state of readiness to accept information which may be transferred into it from the first processor. Moreover, one processor can restart the other after that processor has completed a program. In addition, one processor can give an input-output instruction which is to be executed by the other processor. For example, one processor may give a write instruction to have information contained by the other processor written out onto a magnetic tape. That same controlling processor can subsequently give a read instruction to have the same information read from the magnetic tape back into its own memory for immediate use. Thus one processor can effectively make use of the data stored in the other processor's memory. Conversely, one processor could give a set of instructions which will result in the transformation of data from its memory into the other processor. For this type of operation the programs in the two processors must be coordinated. Some circuits are built into the MOBIDIC B system to direct such traffic bwtween the processors and avoid any uncertainty as to the direction of information flow between them.

Full utilization of the "built-in" duplexing capabilities of MOBIDIC B should provide a challenge to the imagination and foresight of programmers. Many

programs could be written to take advantages of these duplexing facilities. For example, one processor could enter into a different program as a result of the decisions made by the other processor. Also, one processor could take over the other's task if it discovered that the other processor was either overloaded or incapacitated.

Marginal Check and Control Console

An automatic marginal checking system is incorporated in MOBIDIC B. The checking circuit is so designed that the bias voltage in each row of every rack in the computer is modified by a predetermined amount. While the bias voltage of the row is maintained at this changed value, a simple check program, which is stored in the computer, will be run through once. The result of this program can be observed, an error condition will be indicated by a pilot light on the console. All rows are automatically tested in succession in such a manner. It is possible to bypass some racks in the computer so that marginal voltages are not applied and checking is not performed on them. This is necessary to enable one processor and some associated input-output equipment to be in continuous operation while the other processor is undergoing test.

The control console for MOBIDIC is also duplexed. It consists of two independent and identical consoles assembled side by side. Each console is permanently connected to one processor and thus communicates only with its assigned processor. For ease of operation, each control console is divided into 6 horizontal areas. At the very top of the console is located the marginal check voltage control. Immediately below this area is the control for the power to the computer. The master clock selector is also located in this area. The display register is situated next in line, extending completely across the console. This is a full length indicating light register which is used to display the contents of any register or memory location selected by the operator. The area below holds the controls for the flip-flop and error detection. Directly beneath are the controls for the insertion of manual instructions. Initiation control for the computer such as start, halt, and single pulse, are laid out in the bottom row on the control console.

Inasmuch as the control consoles are assigned to their respective processors, operation of one console is entirely independent from the other. However, since the two consoles are located side by side, the operator can easily observe the status of both processors, allowing convenient control of both processors during duplex operations.

Concluding Remarks

Since there are only two physical working registers in each central processor, connections from the central processor to the in-out system are made only through the memory register. Traffic coming in and out of the memory as well as going to and from the in-out system frequently create logical problems. Resolution of these logical problems results in a slight reduction of computation speed.

The internal duplexing features introduced in MOBIDIC B represent a new approach in the design of a large scale, general purpose data processing system. There will undoubtedly be many areas where such an approach is highly desirable from the standpoint of reliability and economy.

Acknowledgment

Many people have contributed to this project. In particular, Messrs. W. S. Humphrey, Jr., and J. Terzian, who have been directing the system and logical design effort on this project have made numerous suggestions and contributed heavily towards the original concept for this entire system. Mr. G. Rocheleau was instrumental in the detail design of the central processor and the design of duplexing capability in MOBIDIC B.

Discussion

M. Rubinoff: Would you include simultaneous solution of the same problem in what you mean by duplex operation?

Mr. Chao: Yes I would. For instance, you can have two processors operating simultaneously, each doing a part of the entire problem, or you can have both processors operating on the same problem and duplicating the computation for reason of reliability.

Mr. Rubinoff: You can make comparisons?

Mr. Chao: Yes, you can make comparisons at the end, or any convenient intermediate point. Note that a simple yes or no type of comparison could be made through the mutual monitoring facilities built into the hardware. For more elaborate comparison, data would have to be transfered over through the input-output device.

C. W. Einolf (IBM): Would you discuss mass memory more thoroughly? Is it a single disc or many? Is it Sylvania designed or built by others?

Mr. Chao: The mass memory consists of eight large discs, 34½ inches in diameter. Both sides of the discs are used. There is a total of 4,096 tracks. The recording and reading is done in serial track by track. You can consider the entire storage to be a looped spiral. In other words the track sequence is continuous. If you go down to the 4,096th track, for the next increment you will get number one track again. Sylvania is collaborating with a contractor in the design of the mass memory; the contractor supplies the discs and we design the necessary electronic circuits.

J. Reitman (Teleregister): Can the MOBIDIC B system be extended to 3 or 4 processors? If so, is there a limit?

Mr. Chao: The logical problems involved in duplexing are not trivial. Extending the number of processors beyond two and tying them all to the same system bus would be undoubtedly a little tougher. There must be a limit somewhere. We have not yet investigated this limit.

G. Gaschnig (RCA): What is the speed of the core memory?

Mr. Chao: 8 microseconds read-write cycle.

W. Towles (Martin Co.): What is the clock frequency and what type of logic circuitry is used?

Mr. Chao: Clock frequency is 1 megacycle. The transistor inverter logic is used.

Mr. Towles: Do the core memories operate reliably at the high temperatures required of a military computer?

Mr. Chao: Yes, it has to. This entire system is designed to meet military specifications.

Mr. Rubinoff: Well, I think the question is which one?

Mr. Chao: Temperature compensation technique used in the memory circuit will be discussed in a paper tomorrow.

S. Levine (Teleregister): What error checking facilities are included and what is the expected undetected error rate of each processor?

Mr. Chao: The automatic error checking facility we have is the parity bit error indication. This gives you single error detection.

Mr. Rubinoff: Any odd number?

Mr. Chao: Yes.

Mr. Rubinoff: What is the suspected undetected rate?

Mr. Chao: We haven't looked into that.

Mr. Levine: Is interlocking automatic or programmed when both processors try to get to the same device?

Mr. Chao: They are automatically interlocked so that whichever comes first will get it.

R. E. Warner (Ford Instrument): If processor No. 2 determines that processor No. 1 is in error, how are you sure that processor No. 2 is itself not in error while processor No. 1 is actually correct?

Mr. Chao: I think we shall have to rely on the statistics. This is a double-error.

W. Buchholz (IBM): The numerical data word appears to have one more bit, the sign, than any other word. How is this sign bit transferred to and from magnetic tape? Does the tape control have to know whether a word is numerical or not?

Mr. Chao: The tape is controlled by the converter. In the case of numerical data, the sign bit is taken out and composed into a character. Therefore, for interpret sign mode of operation, you have 7 characters instead of 6 for each MOBIDIC word.

E. B. Cohen (Auerbach Electronics): How are the built-in subroutines constructed? How is return from these built-in subroutines effected?

Mr. Chao: The subroutine is written as program using the mechanized instructions. Whenever a subroutine instruction is encountered, the accumulator and the program counter are automatically stored by the logic circuit. They have to be saved because these two registers are used in the subroutine. Subsequently, the logic circuit will automatically transfer the program into the correct subroutine. Upon completion of the subroutine, all you have to do is to bring back these registers and return to the main program.