THE engineering design of the LARC solid-state computer was a monumental challenge. The initial job in the LARC development program consisted of determining the type of circuitry and logic that would meet the speed requirements, which called for a decimal self-checking adder which could add two 11-digit numbers in 1 microsecond and multiply them in 8 microseconds. The basic machine timing was determined by the multiplication instruction; it requires 11 additions of partial products, several cycles devoted to the generation of multiples of the multiplicand and a few more cycles for handling signs and transfer of results to a register. Sixteen operations have to be accomplished in 8 microseconds; thus the basic repetition rate is 2 megacycles or, in other terms, information must be capable of entering the arithmetic circuits every half microsecond.

We realized that the circuitry had to be faster than anything then devised in order to meet these speed specifications. A program was set up to consider all conceivable variations of solid-state circuits in order to select the best circuit. Our definition of “best circuit” was primarily based on a figure-of-merit formula given in Fig. 1. The formula is based on the following considerations: The more drives or output a circuit has, the more logically useful it is. Similarly, the more logical levels included within the circuitry, the better it is. In particular, an AND/OR circuit is logically more powerful than an OR circuit by itself. (Drives) (Logic Levels) (Repetition Rate) (Transit Time) (Cost)

On the other hand, the greater the transit time (electrical delay plus a portion of the rise time) the poorer the circuit. Also, the number of times the circuit can be used per second is an important factor that determines how many will be needed for a given task. A circuit having a long recovery time, such as a blocking oscillator, would be poor. Finally, the lower the cost of the components, the greater the figure of merit. Reliability is also reflected into the figure of merit through the cost factor. In general, the lower the cost, the fewer the components involved and the greater the reliability. As a first approximation, all factors in the equation are assumed equally weighted, but it should be remembered that low transit time per logical level was what was wanted most, but not at too high a price for the amount of equipment involved. If for some reason one factor is considered more important than another it can have a multiplier or exponent applied. On this basis the circuit shown in Fig. 2 was selected. If the figure of merit is normalized at 100 for the circuit selected, it may be compared to others, such as the DCTL with 2.8 or the transistor-transformer combination having a figure of merit of 4.1, or a circuit similar to Fig. 2 with a feedback diode to prevent saturation. This latter combination produced a figure of merit of 52.5. The circuit in Fig. 2 is recognized as a basic AND inverter or OR inverter circuit. The surface-barrier transistor was selected for use with this basic LARC circuit because it was the only high-speed transistor that was reliable and in mass production at the time of circuit design.

Diodes are used to perform logical operations, and transistors perform the negating and amplifying function. The same diode network acts either as an AND circuit or an OR circuit, depending upon the polarity of the incoming signal. When used as an AND circuit, all inputs must be low (−3v) in order for the transistor to turn on. When used as an OR circuit, any input going high (On) will act to turn the transistor off. The transistor is operated into saturation and at cutoff; therefore, the output swings from −3 to approximately 0 volts, and is directly coupled to the next circuit. Effective switching occurs during the first ½ volt of the transition. The resistor network $R_1$, $R_2$, and $R_3$ provides the proper transformation of DC levels to the base of the transistor. The capacitor, $C_1$, acts to supply extra current in initially turning the transistor either on or off. $R_4$ is used to provide a minimum load on the circuit, to limit the storage time of the transistor, and also to

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provide current for discharging the stray capacitance. The circuit is designed to accept a fan-in of as many as 13 inputs and is capable of providing 3 full drives output. However, with the use of mutual exclusion (load sharing) it may fan out to several additional places. The maximum output capacity allowed for this circuit is 80 $\mu$A.

Now let us consider how the basic circuit is used to perform logic in LARC. The circuits are used in cascade, so that they form an AND/OR, AND/OR, etc., chain. Ideally, it would be desirable to continue in this fashion. However, pulse timing becomes inaccurate and therefore retiming must occur in certain places. This is accomplished by means of the pulse-former circuit shown in Fig. 3. This circuit permits a logical operation to be performed at its input. The first transistor stage operates a gating network which then selects either a positive or negative timing pulse (90 m$\mu$s, wide) to set or reset the following flip-flop combination. The flip-flop can only be set or reset at precisely-timed one-half microsecond intervals. A chain of logic is depicted in Fig. 4. The sequence is started when pulse-former 1 initiates a transition at one of the timed intervals. The wavefront progresses through the chain of AND/OR circuits where the necessary logical operations take place. The maximum transit time per circuit under worst-case conditions is forty millimicroseconds. Allowing for 9 levels of logic, the wavefront arrives at the timing gate of the second pulse-former 360 millimicroseconds after it leaves the first pulse-former. Since the timing pulse at the second pulse-former is scheduled to arrive in 500 millimicroseconds, the difference of 140 milli-

microseconds is allowed for timing pulse jitter, pulse-former operation and safety factor. Under normal operating conditions the average propagation time of the signal has been found to be 20 millimicroseconds. Thus there is a very large factor of safety in the circuit timing. The circuit transit time corresponds to 25 megacycles. If less than 6.6 levels of logic are employed between pulse-formers, there is the danger of the signal's propagating too fast and arriving at the pulse-former before the previous clock pulse has disappeared. To prevent this, it is necessary to add sufficient delay elements to pad the chain to minimum delay levels. Padding delay has been required in fewer than 10 per cent of the logical chains.

In addition to the basic logical circuit, the pulse-former, and the delay element already mentioned, there are several other high-speed circuits. One is a high-power amplifier capable of producing about 10 times as much current output as the basic circuit which can therefore drive 32 basic circuits. However, this circuit pays for its extra output by consuming 3 levels of delay. Another useful circuit is a scaled-down basic circuit to operate at 1/4 the power level. Thus, one of the basic circuits can drive 9 of the lower-level circuits. The lower-level circuit, however, consumes 1.6 delay levels. The last useful high-speed element is the high-power amplifier coupled with the pulse-former to form a high-power pulse-former.

The fact that LARC circuitry is clocked allows the use of what is called the “pulse-envelope system,” or more familiarly, “non-return-to-zero” (NRZ) logic. If direct-coupled circuitry is used in asynchronous circuits with NRZ logic, two difficulties appear. Either the length of delay through all logical paths must be predicted and be reasonably constant, or a signal from a circuit must be derived to tell when the logic in a chain has been completed. If the former method is used in a parallel computer, there is no advantage over the clocked system.

In the arithmetic circuits, for example, many logical paths operate in parallel. Therefore, if a delay element is to signal when the last of the data has come through, it must have a delay equal to the clock-pulse spacing in a synchronous machine. On the other hand, if the signal itself is used to tell when an operation is completed, there is the problem of discriminating between a normal signal and the “spikes” (switching transients). This is because a gate with one input being turned on at the same time another input is being turned off will, for a finite signal rise-time, allow a spike to come through, as shown in Figs. 5a and 5b.

Now if a return-to-zero or regular pulse system is used there is always a dead space between signals. All signals return to zero during this dead interval and avoid the spike problem. However, the speed at
which pulses can now be put through the circuit (for equal rise and fall time) will be halved because of twice the number of transistors. Since LARC transistor circuit delays are quite stable, less than a two-to-one timing margin is allowed in the clocked circuits. Thus the necessity of using return-to-zero signals would decrease the data rate by more than asynchronous operation would increase it.

Asynchronous operation not only requires more equipment and has no apparent speed advantage, but makes testing and maintenance more difficult, since no definite points to trigger an oscilloscope can be found: timing depends on actual circuit parameters and the actual signals present.

A large number of logical configurations involving adders, complementers, and other devices were examined. Methods of multiplication and division were chosen carefully, not just on the basis of speed, but the circuits were examined to find out how many drives an individual element need provide so that an overall minimization of the speed through a chain of these elements might be made. Since the product of current gain times the band width for a given transistor is normally constant, it is possible to estimate the delay through a network, given the number of drives required at each level.

With a simple fan-out network, this optimum occurs with three drives; however, there is no assurance that this is the optimum for an adder network. Although it was suspected that the same limitations were probably true in actual circuits, many circuits were carefully laid out and it was shown that not only were three drives adequate, but such an arrange-
purposes have all diodes and transistors in place. Card dimensions are approximately $3\frac{1}{2}''$ by $9''$. This shape was chosen to obtain the necessary volume for housing the components. Female contacts are used on the card connector so that there is no possibility of damage which might occur if male contacts had been used. The wires observed on the package serve the function of providing connection between the floating female contacts and the printed circuit wiring. Lower stray capacitances are also achieved and input-output printed-circuit wire bottlenecks is reduced. The male connectors are packaged extremely close in the basic modules which go together to form the backboard. Fig. 7 is a photograph of a module backboard before wiring. The degree of packing efficiency is very high when it is realized that 88 per cent of the backboard wiring area is composed of connectors. As a consequence of this, and the close packing of contacts, there are over 6000 wire terminations per square foot. Reducing the backboard area in this way has allowed the use of wires sufficiently short so that no special line-driving elements are necessary. It was necessary to leave small spaces (30 mils) between connectors to permit a small amount of air flow for cooling purposes. All wiring on the backboard is done with taper pins. With this high a wiring density, as shown in Fig. 8, it becomes impractical to consider soldered or wire-wrapped connections. The connectors are color coded to make the job of terminal identification much easier for the wiremen. Each terminal on the connector is bifurcated and appears as two taper-pin holes so that it is possible to propagate the chains of wires without using auxiliary tie-points. The wiring is extremely dense and piles up to a depth of several inches over most of the backboard. Throughout the development phases of the program, accessibility to the backboard was a matter of gravest concern, since it was impossible to accurately predict or simulate actual backboard wiring buildup. We have since installed many thousands of wiring changes and have fully proven that the wiring technique is indeed practical. We have developed new technology and new tools for working with this new high wiring density. Fig. 9 is a photograph of special tools, which
include long armed taper pin inserters and extractors, pin point light sources, and a "Borescope," originally developed for examining the inside of a gun barrel, but proven effective for penetrating the mass of backboard wire and giving the wiremen a close-up view of the connector. In order to reduce the congestion on the backboard, very fine steel-core copper wire was used with a thin teflon insulation. The physical strength of size 30 steel-core wire is approximately equal to copper wire of twice the cross sectional area. Reduction in wire size not only helped to reduce congestion but also produced a necessary reduction in the stray wiring capacitance.

One of the more serious problems that could occur with many thousands of transistor circuits operating simultaneously is that of crosstalk and other noises being coupled into the transistor circuits. Crosstalk effects were calculated as much as was possible and further experimentally checked in the laboratory. To prevent crosstalk due to coupling between backboard wires, twisted pair is used for any wire lengths greater than about nine inches. Although tests indicate that twice this length could be used under worst tolerance conditions, approximately 23 per cent of the backboard wires are twisted pair. The twisted pair is composed of very fine steel-core teflon-insulated wires with a capacitance of 8 to 9 μF per foot. A network of taper-pin ground straps is provided at each 1/2-inch interval over the entire backboard to form a ground plane. The twisted-pair ground wires terminate at these ground straps. All framework elements of the module carrying ground currents are gold-plated so that the contact resistance between abutting structural members is low and stable over a long period of time, despite atmospheric conditions. Common coupling on the DC voltage lines is minimized by the use of very wide strip transmission lines having extremely low impedances. Strip transmission lines are mounted in vertical columns behind the backboard. These lines have an impedance in the region of 30 milliohms (.03 ohms). Timing-pulse signals to pulse-formers are also available on similar strip transmission lines.

Usually, three DC voltages are distributed to the printed-circuit packages through the strip transmission lines. Up to 6 voltages are available for other miscellaneous card types.

The task of laying out the backboard wiring and positioning the various circuits in such a way as to avoid too much wiring load on any one circuit, as well as the problem of keeping an inventory of all circuit cards, would have been impractical had this not been accomplished by processing the data on a Univaac® data-processing system. Thirty-five different categories of information, as well as complete production-wiring tables, were generated by the Univaac system to supply necessary information for production, maintenance, manufacturing inventory, and engineering test of LARC. For example, printouts were obtained on wires sorted by lengths, potentially bad cases of stray capacity or crosstalk, spare diode and circuit positions, checks on certain types of logical errors, and general data vital for testing and maintenance. All logical revisions which were made during the test period were handled in this automated and systematic manner.

The automated backboard program guaranteed that wiring changes could be made without fear of overlooking any of the myriad of details involved in the change. Fig. 10 shows one page of a printout of the backboard wiring table.

Solid-state power supplies are used throughout the system. Each cabinet has its own set of power supplies and controls, so that lead lengths between card library and power supply can be kept to a minimum. The lead impedances between power supplies and the card library are kept low by the use of bus bars with electrolytic filter-capacitors distributed along the length of the bars. The supplies are all voltage-regulated, either by shunt transistor regulators or, in the case of the very high current supplies, transistor-driven magnetic amplifiers. The size, cost and time of response of the power supplies have been reduced by the use of 400-cycle 3-phase input power derived from a motor-alternator set. The motor-alternator also has the advantage of providing complete line isolation and will produce full output even though power line "dropouts" occur for as long as 3 seconds. The power supply design has proven extremely reliable, with voltage regulation much better than the specified 2 per cent.

A major virtue of the circuitry, not found in many high-speed computer circuits, is its adaptability to a simple and effective marginal-checking system. Varying the collector-return voltage has proven to be an effective way of determining the beta margins of the circuit. Fig. 11 is an actual plot, showing how the
### Wiring Table for LARC Computing Unit

#### Module 3 to Module 4

<table>
<thead>
<tr>
<th>Line</th>
<th>Type</th>
<th>Color</th>
<th>Length</th>
<th>From Terminal</th>
<th>To Terminal</th>
<th>Length</th>
<th>Wire Checked</th>
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<td>4001 LR Black (00B)</td>
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<td></td>
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<td>4002 LN Orange (13A)</td>
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<td></td>
</tr>
<tr>
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<td>3803 LN Orange (23B)</td>
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<td></td>
</tr>
<tr>
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<td>Green</td>
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<td>3804 LN White (31A)</td>
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<td></td>
<td></td>
</tr>
<tr>
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<td>3805 LN Black (10B)</td>
<td>4005 LN Yellow (04A)</td>
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<td></td>
</tr>
<tr>
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<td>3807 LN Violet (00B)</td>
<td>4001 LN Yellow (24B)</td>
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<td></td>
</tr>
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<td>3807 LN Black (26A)</td>
<td>4002 LN Blue (17B)</td>
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</tr>
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<td>4001 LN Brown (00B)</td>
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<td></td>
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<td>4002 LN Orange (03B)</td>
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<td></td>
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<td>4002 LN Black (16B)</td>
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</tr>
<tr>
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</tr>
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<td>4007 LN Black (20B)</td>
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<td></td>
<td></td>
</tr>
<tr>
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<td>White</td>
<td>5.5</td>
<td>3806 LN White (21A)</td>
<td>4006 LN Yellow (14B)</td>
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</tr>
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<td>4006 LN Brown (10B)</td>
<td></td>
<td></td>
</tr>
<tr>
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<td>Green</td>
<td>5.5</td>
<td>3801 LN Orange (03A)</td>
<td>4006 LN Orange (03B)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>Single</td>
<td>Yellow</td>
<td>5.5</td>
<td>3802 LN Violet (18A)</td>
<td>4006 LN Yellow (24B)</td>
<td></td>
<td></td>
</tr>
<tr>
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<td>White</td>
<td>6.0</td>
<td>3803 LN Blue (17B)</td>
<td>4007 LN Green (35A)</td>
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<td>Brown</td>
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<tr>
<td>24</td>
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<td>Brown</td>
<td>6.5</td>
<td>3806 LN Black (06A)</td>
<td>4005 LN White (31B)</td>
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</tr>
</tbody>
</table>

Fig. 10.

Collector-return voltage may be varied to determine the beta margin, which is perhaps one of the most variable and critical of the transistor parameters. The extremely difficult problem of switching individual portions of the very low-impedance voltage-distribution system has been avoided by varying the voltage over the whole unit rather than in a given area. The location of a weak circuit is indicated logically, by error detecting circuits which are located at strategic points throughout the logic of the machine. Thus almost no equipment not already present for continuous checking is necessary to provide very effective marginal checking. An overall marginal check can be performed simply by flipping a switch at the engineer's console while an engineering-test routine is being run on the unit. A comprehensive voltage-monitoring system is used to detect the fact that a particular power-supply voltage is drifting out of tolerance. This fact causes visual and audible indications before a voltage drifts far enough out of tolerance to cause actual errors. The voltage monitor makes use of solid-state elements.

The Computing Unit and Processor are each supplied with a system of fast magnetic registers which are composed of fast-switching tape-wound cores having a read-regenerate or clear-write cycle of 1 microsecond. The fast-register core consists of 4 wraps of 1/2 mil thick, 1/2 wide, 4-79 molybdenum permalloy tape on a 50-mil diameter stainless-steel bobbin and has a read, a write, and an output winding. The register uses one core and diode per bit and is organized on a word-selected basis. As employed in the Computing Unit, information write-in or read-out is done in 60-bit parallel form. Fig. 12 is a photograph of a fast-register package. The cores and diodes are contained in the small rectangular boxes and are

![Photo of fast-register package](http://www.computerhistory.org)
arranged in a $26 \times 30$ array. Two of these packages are used to form 26 registers of 60-bit storage. More of these packages may be plugged into the Computing Unit to make available a maximum of 99 registers that can be used interchangeably for indexing or arithmetic operations.

To carry out the logical operations in parallel fashion, large quantities of circuits are required. To present some idea of magnitude, a few of the statistics will be listed: 8800 printed circuit cards are used in the basic system, with approximately 3700 in the Computing Unit, 3200 in the Processor and 1800 in the memory. This represents a total of 62,000 transistors in the entire typical system, with approximately 57,000 of them being surface-barrier transistors. 28,000 transistors are used in the Com­puter Unit alone. The number of logical diodes in the system is approximately 2.8 times the number of transistors. 75,000 wires are used on the backboard of the Computing Unit.

With these large quantities of components used in the system, it is quite obvious that reliability is a major problem and, therefore, a big part of the LARC development program was concerned with component reliability. Many of the basic component selections were made on the basis of reliability rather than cost. All components used in the system were subjected to extensive reliability tests. The resistors used in the circuitry, for example, are of the $\frac{1}{2}$ watt size, even though circuit dissipation is in the milliwatt region. The $\frac{1}{2}$ watt resistor available at the start of the project proved to be much superior to the smaller wattage sizes. A large engineering effort was required to achieve the high reliability obtained in the LARC printed-circuit card connector. The contact pressures are accurately designed to be in the 4- to 6-ounce range per contact. The use of electro-polishing and 200 micro-inches of gold permits the connector to be withdrawn and inserted 400 times while still retaining gold both on the male and female contact area. This is an important point, in view of the low voltage and current levels encountered. All circuits are designed to work under worst-tolerance conditions assuming 4 per cent variation in DC supply voltages, a 3-per cent variation in the value of the resistors, and the end-of-life transistor beta. Three units of beta over the end-of-life beta required are specified for new transistors. For example, for a transistor driving 3 loads, an old-age beta of 9 is required; a transistor with a beta of 12 minimum is initially inserted in the circuit. Under nominal tolerance conditions, the circuit will function even if the beta drops to 6. The most pessimistic calculations of reliability have predicted a mean-error-free time of at least 11 hours, which is 3 hours beyond that called for by the specifications. Typical power requirements of the system are 15 KVA of 400-cycle power for the Computing Unit, 56 KVA for each memory unit, and 18 KVA for the Processor. The power factor is .5 because of the type of regulated power supplies employed. Most of this power is actually dissipated within the power supplies.

Each unit of the system has its own cooling equipment built into the base of the unit. A heat exchange and blower system circulate $75^\circ$F maximum-temperature air up the backboard and through the card library; the air then returns through the front side of the machine to the base area, thus forming a closed-circuit path. The circuits will operate over a much wider temperature range, but internal cooling is used to guarantee long life and reliability. Operation is reliable over a room temperature range of 32 to $110^\circ$F.

The LARC system is being readied for the customer acceptance test. All units of the system are functioning. The Computing Unit, in conjunction with the memory, has been running test routines for many months. Although the overall long-term reliability data on the system is not yet available, preliminary information is very satisfactory. Runs of about 12 hours have yielded one or no intermittent errors. Fortunately, the very few failures encountered thus far have been of the catastrophic variety, such as open or shorted components (probably due to abuse during testing) rather than a change in parameter value which leads to marginal operation and accompanying difficulty in isolation. It is extremely gratifying that no circuit redesign of any sort has been found necessary since the commencement of test. This has led to an unusually rapid testing of the overall system. The efforts put into very thorough engineering beforehand have paid off handsomely.

Many people were involved in making the LARC program a success, and it would be impossible to list them all by name. Recognition must be granted to all of them for their part in this major engineering achievement.

**DISCUSSION**

*S. Levine (Teleregister):* What is the expected LARC reliability: i.e., mean free time to failure, fault location time, mean repair time of main processor and sub-systems? What size of maintenance crew do you expect to require for a typical installation operating 24 hours a day, seven days a week?

*Mr. Lukoff:* Well, we have calculated the mean free error time using reliability figures provided to us by our component engineering groups and by Bell Telephone, RCA, and so on. The mean free error time is predicted as at least 11 hours which is three hours beyond that called for in the LARC contract specifications, which ask for an eight-hour mean free error time.

*Mr. Eckert:* The few runs we have made so far are better than this. We have made a few runs of 12 hours during the course of system testing, and it has actually been better than this. We haven’t run enough to know the ultimate mean free time to failure.

*Mr. Lukoff:* The repair time on a card would be, say, two minutes to replace a diode or transistor. We have automatic package-checking equipment that checks the package under dynamic operating conditions. It measures the transit time to within 3 millimicroseconds and
From the collection of the Computer History Museum (www.computerhistory.org)

Lukoff, Spandorfer and Lee: Design of Univac-LARC System: II

pretty well down to the component that has to be replaced. This can
done very rapidly. We have a supply of spare parts the mainte­
nance man is furnished with. He would, of course, replace the defec­tive package in the machine with a good spare package and make the
repair on the bench.

We are presently in the process of developing and refining the
LARC maintenance procedures. However, we believe that mainte­
nance will be easier than with any other machine we have built thus
far because of the packaging techniques, and because of the large
amount of checking which permits logical isolation of the circuit.

On the maintenance crew I would expect it to be of the same order
of magnitude as it is for any other computer in the field.

J. Capobianco (Hughes): What type of logic diode was used? What
are its transient specifications?

Mr. Lukoff: The diode is a point-contact diode selected for its high
speed capabilities. Also, the forward drop was an important consider­

ation in the direct coupled circuitry. I don’t remember the exact
specification for speed but it is a fast diode.

Mr. Eckert: It is about two or three times faster than the usual run­
of-the-mill gold bonded diode. Actually we have two types of diodes,
gold bonded and plated tungsten. We have four or five different sup­
pliers who could make such a diode. It is a better diode than the one
you go out and buy over the counter. It is one manufactured for well
under a dollar.

V. Enstein (Brooks Research): What method of switching is used to
switch between the various drums? What significance is attached to
the two different chairs for the operator and the engineer?

Mr. Lukoff: Purely esthetic, in answer to the second question. In
answer to the first, we use relay switching cabinets.

Mr. Eckert: We have plenty of time to switch because you are really
stripping one drum while you are reeling off the other.

Mrs. J. Schot (D. Taylor Model Basin): What is the maximum reli­
able pulse density of the LARC tape units? In other words, is it pos­
tible to store two drum loads on one reel of tape?

Mr. Eckert: We are using standard Univac, which packs 250 to the
inch. We have experimental tape which goes much higher. As I said,
we will put either these tape units or competitive tape units on the
machine to suit the customer.

G. Neuman (Magnavox): With the large number of transistors used,
what percentage of rejects did you have in construction?

Mr. Eckert: About 10 percent, wasn’t it?

Mr. Lukoff: We knew we would have about 6 percent rejection on
transistors because we bought the complete line of transistors from the
manufacturer, and we knew some would not meet our specifica­
tions.

Mr. Eckert: We buy transistors to normal specifications and buy
everything on the line and then throw out about 6 percent due to low
current. Again this is no problem.

D. Hammel (RCA): What are the possibilities of a third computer
operating in the LARC system?

Mr. Eckert: That is easy. It is not designed for it. It doesn’t have
enough time slots.

P. J. Scola (GE): Do you use diagnostic programs? What percentage
of the faults do they find? Average time to locate fault?

Mr. Lukoff: We can only partly answer by saying we definitely plan
to use diagnostic programs but have not had the opportunity to fully
explore their potential in the computer yet.

Mr. Eckert: I suspect you could ask Mr. Tonik after the conference
session.

M. Sendrow (RCA): Is there any way of loading the drums from any
external media? If so, what media and how?

Mr. Eckert: Yes, they can be loaded from tape units, by punch cards,
card readers, through the core memory. You could, if you wanted,
from keyboards, but it would take all your life.

J. Katz (GE): How many wiring mistakes in the backboard were
traceable to malfunctions in the data processing program?

Mr. Lukoff: None.

Mr. Eckert: Most of the wiring errors we found in the backboard were
either production errors or due to logical design errors. There were
lots of errors, but there have been on every machine I have seen.

W. C. Mann (Westinghouse): About what percentage of the back­
board connections are used?

Mr. Lukoff: It is very high. I don’t remember the exact figure, but it
is in the order of 75 percent.

Mr. Eckert: As far as correcting these, these logical errors, that is the
reason for the long handled tongs.

G. A. Sellers (Bell Labs.): Please repeat the characteristics of the
high-speed microfilm printer. Is it going to be commercially available?

Mr. Eckert: Yes, it is commercially available. It prints at 20,000 char­
acters a second. I think you can produce it on a polaroid, too, if you
want a single frame and print points at this speed. It could print at
a somewhat higher speed, but we didn’t choose to. So it makes a good
plotter.

F. P. Jenny (IBM): How do you differentiate between errors in the
error detection system and the operational system?

Mr. Lukoff: The error detection circuits are not distinguished from
the computer circuits proper. Nobody watches the watcher. A de­
tected solid error is to be repaired regardless of source. We ignore the
possibility of a double failure over a short time period and employ
error generating routines periodically to check the operation of the
circuit. In some cases error insert switches have been pro­
vided where input/output equipment is involved.

Mr. Eckert: The machine doesn’t necessarily stop when it makes an
error. It is rigged up so it can go into a routine and try something
over with different conditions. After a certain number of times, it
finally stops. When you have an intermittent error the frequency may
become high enough that you want to service it.

T. Digan (IBM): How do you marginal check the 170,000 diodes?

Mr. Lukoff: The diodes are marginally checked along with the rest of
the circuits. There is just one marginal check test of circuits, not able
to find if the transistors are low or voltages are out of tolerance or
high drop in the diode or the diodes become slow.

Mr. Eckert: You see, we are satisfied to find out which group of cir­
cuits the fault is located in. Then we find out within three diodes or
resistors which is bad. It is an overall clump test, so to speak.

Mr. Thomas (MH): What automatic programming systems are
available for LARC? Do they include special features to aid in the
effective simultaneous use of the several computing units?

Mr. Lukoff: At the present time we are planning a complete assembly
system and a compiler system for LARC to use the argol language.
There will probably be more automatic program work done in the
future although we can’t say much about this at the moment.

T. Gilmer (ITT Federal): You have indicated an unusually short time
in test for LARC. Can you give an indication of the elapsed time
and the number of crews working?

Mr. Lukoff: The processor unit, which was the last one to go into test,
has been in test for approximately five or six months, and it is just
about completed. I think this is very, very short for the number of
circuits involved and for the complexity of the machine.

Mr. Eckert: This is done on three shifts, and, of course, some shifts
are missed now and then for holidays and other reasons.

M. Relis (Curtiss-Wright): What transistor is used in the gate­
inverter?

Mr. Eckert: Philco surface barrier transistor, although it differs in
that a slightly lower resistivity and a slightly different size of ger­
mium is used. Other than that it is a regular SBT transistor.

From the collection of the Computer History Museum (www.computerhistory.org)
G. E. Saltus (BTL): What maximum logical fan-out and fan-in are allowed in the basic circuit?

Mr. Lukoff: A maximum of 13 fan-in for basic circuits and a fan-out of 3 but more places are sometimes allowed because of load-sharing.

Mr. Eckert: You hook up to 10 in some cases, but it only drives 3 due to mutual-exclusion. There are some places where you could get more load by taking the dummy load transistor off. We do that only in the memory.

P. W. Core (IBM): Can both arithmetic computers perform operations in the times quoted simultaneously?

Mr. Eckert: Yes.

R. Adams (DATAmatic): Are there any further requirements for other than twisted pair for those over 9 inches? Specifically I am thinking of termination requirements or coaxial runs.

Mr. Lukoff: There are no terminations required within the main units, but there is still a maximum length; that is, we must not exceed the micro-microfared capacity units. You can't allow longer wirelength for a circuit to drive or else it will take more than its allotted delay level.

Mr. Eckert: Actually we computed — we had to compute — everything twisted above 15. We actually twisted everything over 9 inches, and it amounted to 30 percent of the wire.

M. Lavel: Are there any tubes used in the LARC?

Mr. Eckert: Yes, to get the fairly sizable clock powers. At the time we designed there weren't suitable transistors, but they probably exist now.

J. E. Veal (RCA): What is the figure of merit of the diode-core registers as compared to your figure of merit for other circuits in the memories?

Mr. Eckert: We didn't design the core register by a figure of merit. We considered several types, and this was the only type we knew how to build. We knew of others, but the development time was long, so they were thrown out.

Miss H. Bein (Philco): What do you mean by a LARC system with 2 computers? Would they be handling different programs and sharing one memory and data processor?

Mr. Eckert: They would share one memory bank, but don't forget a memory bank can have up to 39 functionally independent 2500-word units in it.

Miss R. Pitche (Northeastern Univ. student): Do you use a parity bit? If so, how?

Mr. Eckert: Well, there are extensive uses of parity bits. They are on the tape unit. The code is carefully chosen to cut down the errors. There are parities all over the place.

E. Morenoff (RADC): What factors limit the number of computing units to 2?

Mr. Eckert: The number of time slots and the needs we saw.

E. L. Lawler: Was the program for backboard wiring primarily for record keeping or was some attempt made to optimize the location of the packages and the interconnections between them?

Mr. Eckert: For both of those and also the calculation of loads and various other things. In the inventory class alone there were 35 different types of lists needed.