prove the welfare of human beings. If there is a real reason for promoting this efficiency, it can be none other than the betterment of human living, whether through better defense of the nation, improvement of the standard of living, relief from manual drudgery, or whatever the specific and valid aim.

In pursuing our goals of greater integration and automation by attempting to predict all eventualities and to prearrange solutions, we as systems workers, must never lose sight of this purpose, lest in our enthusiasm we do harm to our real intent. We must assume major responsibility for insuring that every step forward meets the criterion of even greater human contribution all up and down the line, and therefore even greater human dignity. Progress in systems design and automation must always be measured within this larger perspective, and must forever be conditioned, and perhaps even limited, by this governing need.

A Multiload Transfluxor Memory

D. G. HAMMEL†, W. L. MORGAN‡, AND R. D. SIDNAM†

Introduction

IN the field of computing machinery there is an ever-increasing demand for the development of random-access digital memory-storage units that operate at higher speeds and provide greater storage capacities. In 1951 a digital memory-storage unit that had a capacity of 1000 words and performed the basic memory cycle in about 200 μsec was quite sufficient to satisfy the needs of a large-scale data-processing system. Today memory units of large-scale data-processing systems are being designed to provide as much as 90,000 words of storage capacity and to perform the basic memory cycle in about 4 μsec. The trend is obvious, but the means of achieving desired results are often cumbrous.

The development of a superior memory-storage device is presently a major consideration of many prominent research activities. An important feature of the most promising schemes is the ability of the storage device to perform a nondestructive readout. This means that the state of the storage device is not destroyed whenever a readout is performed. This is not the case with present-day magnetic core memories which destroy the stored information when the core is read, and consequently require that the information be written back into the memory if retention is desired. This in effect gives the nondestructive storage medium a 2:1 speed advantage over the destructive storage device.

The read/write speeds of the memories being developed with present-day techniques are approaching their maximum, and any further increases can be achieved only with decreased reliability and increased costs. These memories are capable of executing only one access at a time and therefore restrict the digital computers to functioning sequentially. The ability of a memory to perform more than one access simultaneously would be a major advancement in the computer field; this would be equivalent to increasing the read/write speed of the memory cycle. But a much more significant aspect to this mode of operation is that it would make possible the practical realization of truly parallel computers, computers capable of simultaneously and independently sharing the same memory or memories and hence able to communicate at the computer speed. A storage system which holds promise of fulfilling all these desirable features is a multiload transfluxor memory.

The multiload transfluxor is a multiapertured magnetic memory element employing the same type of high-remanent ferrite used in the ordinary memory cores. Thus the transfluxor is built upon a strong foundation of practical and theoretical ferrite core knowledge. The wealth of experience that has been accumulated during the development and use of coincident current magnetic core memories is applicable. In addition the transfluxor offers many properties heretofore unobtainable.

The Two-Hole Transfluxor Memory

The original Rajchman and Lo transfluxor is a two-hole ferrite core.[1] The following is a brief explanation of the device. (See Fig. 1.)

The large hole is used for the writing operation and the small hole for reading. There are two parts to the writing cycle: a block pulse and a set pulse. The block pulse is a large pulse, either positive or negative, which saturates the entire core in one direction. When the core is blocked, the flux direction on both sides of the small

† RCA, Defense Electronic Products Div., Moorestown, N. J.
‡ RCA, Astro-Electronic Products Div., Princeton, N. J.

[1] A complete explanation of the device may be found in J. A. Rajchman and A. W. Lo, "The transfluxor," PROC. IRE, vol. 44, pp. 321–332; March, 1956.

hole is the same [Fig. 1(b)]. The set pulse is a restricted smaller pulse of opposite polarity which reverses a portion of the flux in leg one and all the flux in leg 2. This is the set condition of the core [Fig. 1(c)]. The transfluxor is read by applying sine waves or pulses of alternating polarity to the small hole to sense the presence or absence of a set condition. If the core is set, the following occurs. First, a prime pulse, which produces a clockwise path around the small hole [see Fig. 1(d)], is applied to leg 3. A drive pulse is then applied to leg 3 to produce a counterclockwise flux path. The reversal of the direction of the flux path around the small hole by the prime and drive pulses generates an emf which is sensed by a winding on leg 3 [see Fig. 1(e) and 1(h)]. The set condition of the core and subsequent readout of a sense voltage is the equivalent of writing and reading a "1."

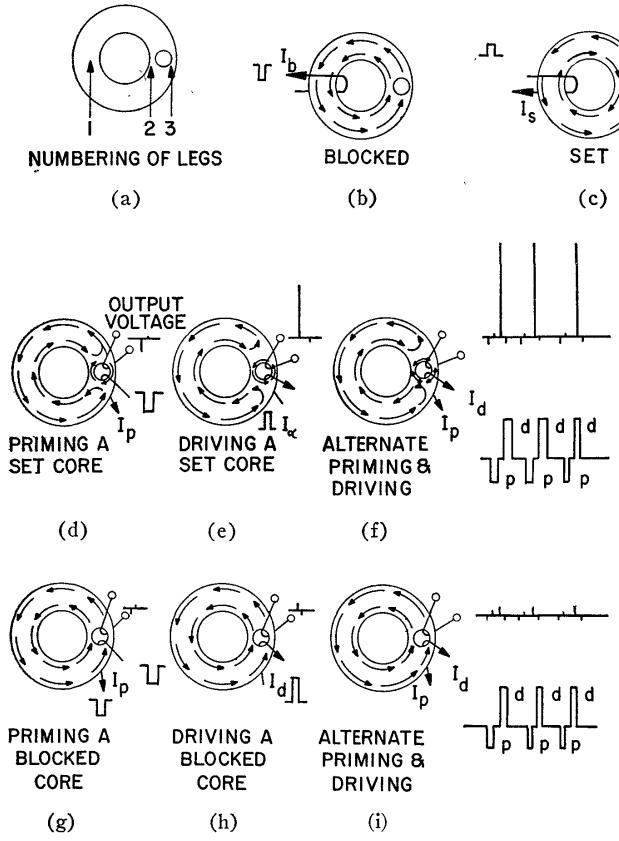

Fig. 1—Transfluxor operation.

In order to write a "0" in the core, the write operation must be modified so that the core remains blocked. This is accomplished by an inhibit winding through the large hole. At the same time the set pulse is applied, a half-current pulse of opposite polarity is applied to the inhibit winding. This half-pulse thus nullifies the set pulse and the core remains blocked. With the transfluxor blocked, the prime-drive pulses will not reverse any flux in the vicinity of the small hole and consequently will not generate any sense voltage [see Fig. 1(g)–1(i)]. Thus the generation or nongeneration of a sense voltage is the equivalent of reading a "1" or a "0" from the core.

The applicable addressing techniques for transfluxor memories are similar to those used for magnetic core memories. Each of the two transfluxor holes may have its own set of selection wires as shown in Fig. 2. Because there are separate addressing systems for both reading and writing, and because there is negligible interaction between aperture signals, it is possible to write in one location of the array while simultaneously reading in another location.

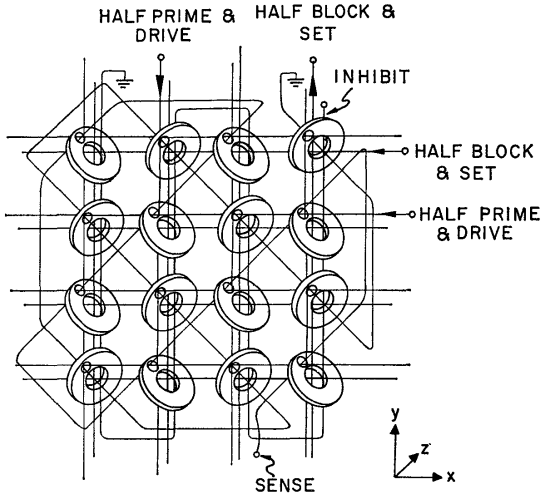

Fig. 2—Coincident current transfluxor array.

An important feature of the transfluxor is its ability to perform a nondestructive readout. This ability of the transfluxor memory system offers significant advantages to the digital computer. Because of the nondestructive nature of the transfluxor, there is no need to restore the transfluxor to its original state after interrogation. This results in the elimination of a major portion of the read/write cycle normally associated with memory systems, and the timing requirements are appreciably simplified. In effect the speed of the memory cycle is increased by approximately 2:1.

This nondestructive read characteristic is also significant in that there are no ruinous effects when a transient error occurs during a read operation. True, the information in a memory location may be read incorrectly due to a transient noise but this does not affect the contents of that memory location since the data do not have to be rewritten from the output. A computer that has a nondestructive memory can easily cope with transient noise by immediately repeating the read operation upon detection of a read error. The ability to read from the memory without destroying its contents is a desirable feature especially in real-time computer applications where the execution of the stored program must be reiterated indefinitely.

The Multiload Transfluxor

One of the attributes of the transfluxor is signal isolation between the windings of the small hole and the large hole. Through the proper physical placement of additional small holes in the ferrite body and a separate set of addressing wires and sense windings in each small hole, it is possible to obtain more than one independent output from the transfluxor without seriously affecting the signal isolation between holes. Thus it is possible to consider three, four, five, or more holes in the transfluxor, offering the designer an extremely versatile memory storage component. This new component is called the multiload transfluxor.

For the purpose of discussion, consider a multiload transfluxor with a large hole and two small holes. If only one of the small holes is used for readout, the performance of the multiload transfluxor is identical to the two-holed transfluxor. A possible configuration of a dual-load transfluxor and its flux patterns with only one of the small holes being pulsed for readout is shown in Fig. 3(a)–3(d).

The cores shown in Fig. 3 are pulsed by the coincident-current address method. This means that two pulses, one on the X wire and one on the Y wire, are needed to supply the total current required to generate the proper flux condition in the core. These flux patterns are nearly the same as those for the more conventional transfluxor. If the prime-drive cycle is simultaneously initiated in both small holes, the resulting flux distributions are shown in Fig. 4(a) and 4(b). Notice that there is minimum interaction between the holes. This permits the timing of the priming and driving pulses for each hole to be independent of the other.

The multiload transfluxor as used in a memory system has a separate set of addressing wires and sense windings in each small hole. Each set of wires is tied to independent address registers and loads. All address registers are capable of addressing randomly any core in the array and any core may be addressed by all the registers. Therefore the information stored in one core may be read out simultaneously to any or all loads, and any number of cores may be read independently into different loads.

With only one large aperture in each multiload transfluxor, there can be only one write/addressing source for each word. This limitation is imposed on the large aperture because each inhibit winding is common to every bit in its memory plane; so it can only represent one addressing source. Of course, multiple writing could be made possible by eliminating the inhibit winding, but this scheme involves many more control circuits. A simple and quite satisfactory method of accomplishing multiple writes is to use a split-memory system. The split-memory system is discussed later in this paper.

There are two techniques for selecting cores or core registers mentioned in this discussion: coincident-current selection and external word-selection (end firing).

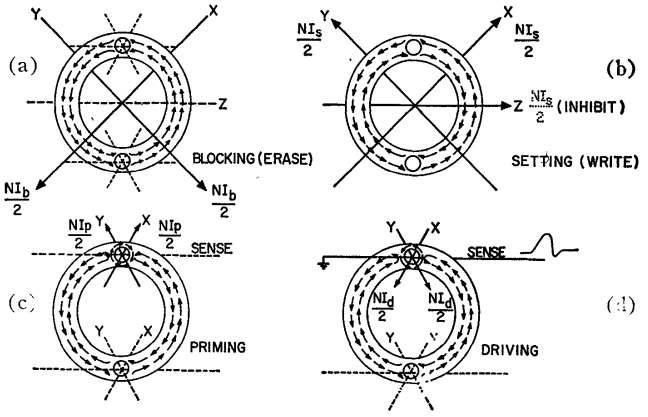

Fig. 3—Flux patterns of a dual-load transfluxor with only one small aperture being pulsed; single-load readout.

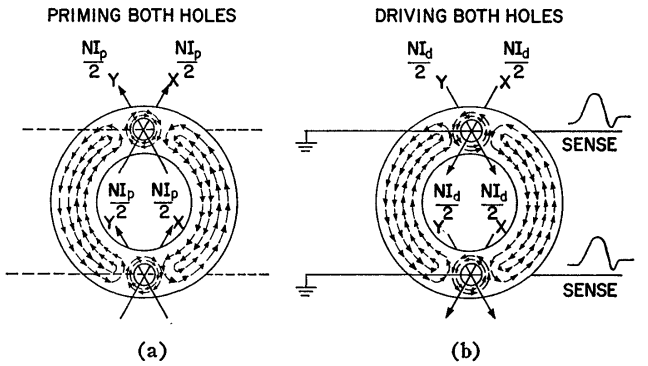

Fig. 4—Flux patterns of a dual-load transfluxor with both small apertures being pulsed; double-load readout.

The coincident-current technique is illustrated in Fig. 5. It is used here to address three cores simultaneously from three independent sources.

The wire leads in the array are designated by a code which describes the addressing source, the addressing axis, and the row or column number of that axis. For instance, $LY3$ indicates that the origin of the lead is the third column in the Y axis of the L addressing source.

In this figure the U addressing source transmits half-current priming signals on the $UX4$ and $UY3$ leads. Accordingly, the upper apertures of cores 41, 42, 44, 45, 13, 23, and 33 all receive half-current pulses, but this half current is not sufficient to significantly disturb the flux pattern around the small aperture. This is a basic requirement of any coincident-current magnetic-core memory. However, core 43 receives half currents on both the UX and UY axis leads and the coincident summing of these currents causes a flux reversal in the vicinity of the small aperture. Thus, core 43, and only core 43, is primed for reading by the U addressing source. Similarly, the L addressing source selects core 13 for reading also, while M addressing source selects core 22 for writing.

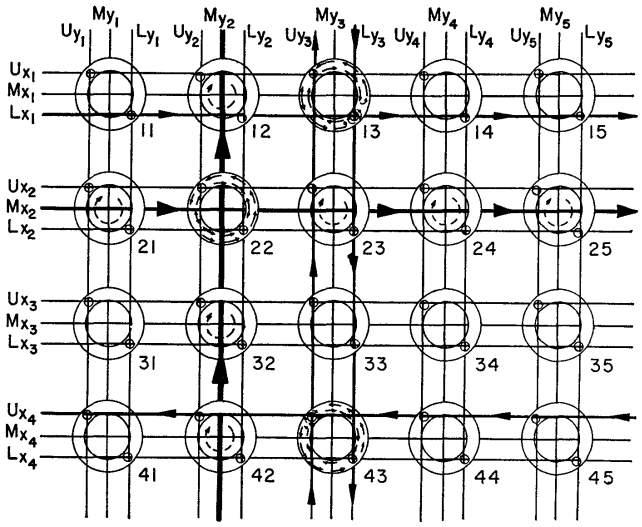

Fig. 5—The effects of simultaneously pulsing three cores; not shown: inhibit wires, sense wires to loads 1 and 2. This is only one plane of the memory.

In contrast to the coincident-current technique of selecting a word by summing the half currents of the X and Y axis leads, the external word-selection technique involves one wire that carries the full current to the selected word. A multiload transfluxor memory using the external word selection is shown in Fig. 6. Memory planes, composed of printed multiload transfluxor plates similar to those of a ferrite-plate memory, are stacked with the selection wires threaded in the word dimension. There are three apertures per bit, with one selection wire through each aperture, thus requiring only 3 physical wires per bit. All other windings can be printed on the ferrite plate, since they are all in the X-Y plane. These printed windings consist of one continuous inhibit winding per plate through each large aperture and two continuous sense windings per plate, one through each upper small aperture and the other through each lower small aperture. The X and Y addressing signals are supplied to an external circuit using either magnetic or transistor switches which provides the gating to select a specific word.

The advantages of this technique are as follows:

1) There is only one selection wire required per hole of a transfluxor. This eases the congestion and reduces the task of threading wires;
2) The noise problem due to the half-current selection pulses is eliminated; and
3) The specifications on the current amplitudes of block and drive pulses are less critical than in the normal array.

The multiload transfluxor for most memory design purposes imposes no additional restrictions than are required for toroidal cores. In fact, other selection methods may prove more advantageous than the ones described.

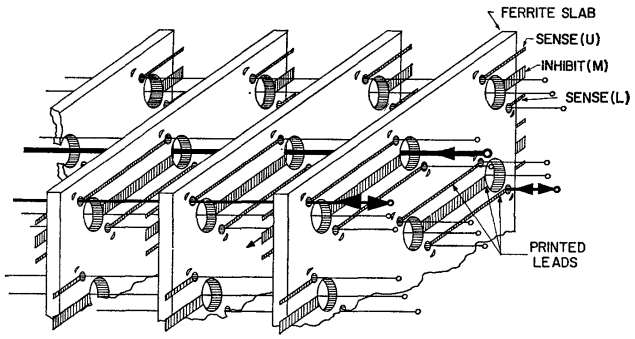

Fig. 6—Switch-driven memory-employing transfluxors.

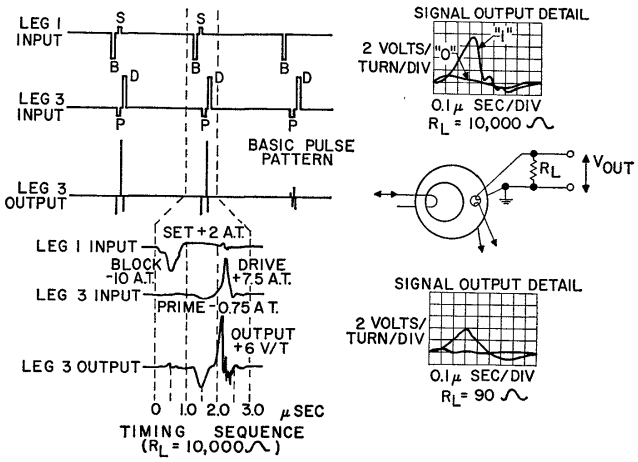

Fig. 7—A test program for a transfluxor of the large size.

Laboratory Test Data

A considerable amount of experience has been gained by RCA in studies on the transfluxor itself and in development of a transfluxor memory for an airborne digital computer. The characteristics of transfluxors which make it ideally suited for high-speed digital memories were laboratory tested. The results are described here briefly; some data and waveforms are shown in Fig. 7.

The test setup used a large core (364-mil O.D.) which requires rather large currents. In practical memories smaller cores will be used with more reasonable currents. A memory is now being constructed using transfluxors with an outside diameter of 200 mils.

The currents used in these test circuits were abnormally large to accentuate certain conditions. The block pulse, for instance, was maintained at 10 amp turns to observe clearly the effect of the set pulse amplitude upon the output. The pulse pattern illustrated in Fig. 7 shows a driven output of 6 volts per turn (peak) with a pulse width of 0.18 μsec (at 50 per cent of pulse amplitude) and a switching time of 0.30 μsec. With such a large output it may be possible to eliminate the sense amplifier in certain applications.

Under laboratory conditions the prime-drive (nondestructive readout) cycle on a single core has been completed within 0.8 μsec. A block-set sequence has been completed in 2.5 μsec. Faster speeds appear to be possible, but could not be observed due to limitations imposed by the testing equipment.

The nondestructive readout properties were tested by setting one core and blocking another. A stream of bipolar (prime and drive) pulses were applied to both cores. After approximately 3,600,000,000 readouts, the outputs were the same as at the start of the test.

One of the problems common to ferrite devices is their temperature dependence. In most memories this problem is avoided by placing the entire core assembly in a temperature-maintained environment such as a 40°C oven. Typically a ±3°C range is maintained. Work has been done by Abbott and Suran[2] and by Bennion and Crane[3] on stabilizing the logical transfluxor for wide temperature variations, but a temperature-maintained oven still appears advisable for coincident current memories.

Computer Memory Applications

There are four basic paths of communication between the memory and other sections of a digital computer:

1) New data are transmitted to the memory from the input unit;
2) Stored data are transmitted from the memory to the central computer for processing;
3) Results data are transmitted to the memory from the central computer;
4) Answer data are transmitted from the memory to the output unit.

In general, present-day computer memories can perform only one of these functions per memory cycle. This means that while the memory is communicating over any one of these basic paths, the other three communication paths are stymied. This inherent interference is a limiting factor in realizing the full operating potential of a digital computer.

The introduction of a computer memory that has the ability to communicate over all four of these paths simultaneously would offer effectively higher speeds of operation and other advantages. Such a memory is now possible through the use of the multiload transfluxor.

Conventional Computer Organization

One suggested organization of a conventional digital computer utilizing a three-hole transfluxor memory is shown in the block diagram of Fig. 8. This memory unit is controlled independently from each of three sources: the output unit, the input unit, and the central computer. The interconnections between these three sources

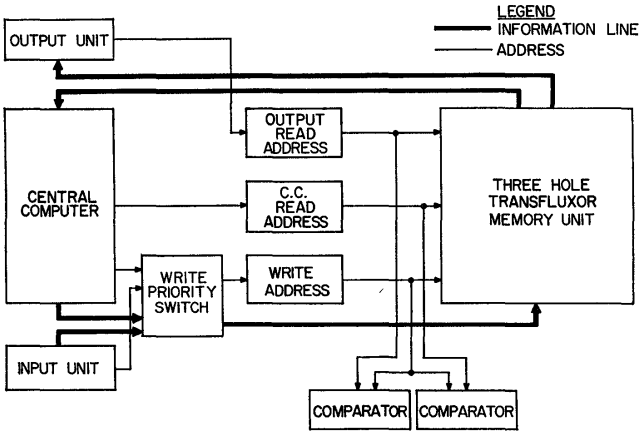

Fig. 8—Computer memory organization using a three-hole transfluxor memory.

and the memory unit are as follows. One of the two small apertures in each transfluxor is used for reading data from the memory to the output unit. The other small aperture in each core is used for reading data from the memory to the central computer. The large aperture in each transfluxor is used to write data into the memory unit from either the input unit or the central computer. Since both of these sources could simultaneously initiate memory-write instructions, a switching and priority unit must be provided to make a decision as to which should take precedence and control the flow of information accordingly. Until the execution of the selected write instruction is completed, the other write instruction is temporarily held up.

The logical operation of this proposed digital computer presents another minor restriction in that it is not permissible to read and write in the same memory location simultaneously. Two comparator checking circuits are required to check for coincidence of like read and write addresses. When like read and write addresses are detected, the procedure is to interrupt the performance of one of the instructions until the other is completed.

Except for these two restrictions, the output unit, the input unit, and the central computer are able to execute all read and write instructions independently, simultaneously, and asynchronously. They can function independently because each source is capable of selecting its own memory location regardless of the performance of the other source. They can function simultaneously because there is no problem of interference when data are read from two memory locations and written into another memory location at the same time. In fact, there is no interference when both read sources simultaneously select the same memory location. They can function asynchronously because good signal isolation makes different timing sources permissible.

Split Memory

The inability of a computer to write into the memory from both the input unit and the central computer

[2] H. W. Abbott and J. J. Suran, "Temperature characteristics of the transfluxor," IRE Trans. on Electron Devices, vol. ED-4, pp. 113–119; April, 1957.
[3] D. R. Bennion and H. D. Crane, "Design and analysis of MAD transfer circuitry," this issue, pp. 21–36.

simultaneously may be solved by another approach more compatible with the philosophy of parallel operations. It is a split-memory system shown in the block diagram of Fig. 9. In this memory system, one portion stores only the data from the input unit and the remaining portion stores only the central computer data. Thus there are effectively two separate memory units for writing information, but only one for reading by the central computer and output unit.

An important point to emphasize here is that the memory can be divided into two or more sections in order to accommodate simultaneous inputs to the memory from two or more sources. This division can be made in such a way as to satisfy the relative storage needs of the inputs. For instance, the memory can be divided so that 40 per cent of it is addressable for writing by the computer, 30 per cent of it is addressable for writing by a tape input, and 30 per cent of it is addressable for writing by a magnetic drum. It is obvious that there is a great number of possible arrangements of such a memory system.

An advantage of this digital computer organization is that there is no interference between the write instructions of the input unit and the central computer and thus no need for a switching and priority unit. As a result there is a definite saving in computer operating time. However, this advantage is gained only at the expense of a somewhat increased demand for memory-storage space and the introduction of two more comparator-checking circuits.

Parallel Operations

Some of the possible uses of a three-hole transfluxor have been given above. Additional small holes in the multiload transfluxor further increase its versatility. The possibility of having many small holes for reading purposes permits the realization of heretofore unachievable system designs. In real-time computer systems, it is desirable to be able to read large quantities of data continuously to output devices without interfering with other memory communications. In a missile control center, for example, there is a need for high-speed printers, tote-board display units, CRT display units, and tape units. Data transmitted to the CRT display units must be renewed at a rate sufficiently fast to eliminate flicker. The tote-board display must be able to exhibit pertinent information that is frequently updated to keep personnel abreast of the happenings. Concurrently, the tape units and high-speed printers must also be able to record in real time. If all of these output devices require access to the same data, the memory must consist of multiload transfluxors which have one small aperture for each output device. However, if the data required for the various output devices are different, the transfluxor memory unit can be split for reading in a manner similar to that discussed previously for writing. In this case, the memory would consist of three-hole transfluxors with one small aperture of each connected to the one applicable output and the other small aperture connected to the central computer. With either configuration there is complete independence of reading by any or all output devices.

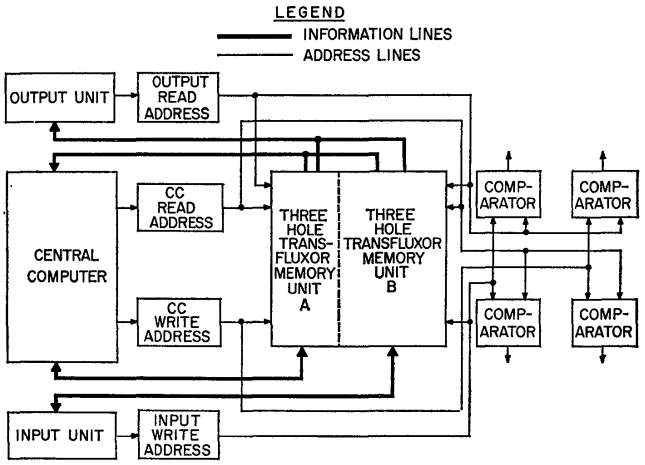

Fig. 9—Split memory system variation of Fig. 8.

The development of the multiload transfluxor memory will make it practical to design and develop central computers that operate on multiple addresses in parallel. This means that instead of the conventional method, which must address each word required by the problem in sequence, all words may be addressed simultaneously in a transfluxor memory. Some novel computer designs based on this principle follow. A computer arithmetic unit could be designed to accept both the augend and addend data simultaneously. Computer logic based on a parallel three-address instruction could permit simultaneous reading of two operands to the arithmetic unit and writing of previous adder results into the memory unit. It is also conceivable to develop a sorting unit that simultaneously accepts and sorts three, four, or more inputs. Such a device would be a welcome addition to business computers where a major per cent of the time is spent sorting.

Common Memory

It is becoming increasingly important in the fields of science, computer checking, and real-time applications, where the speed of computation exceeds that permitted by one high-speed computer, to devise systems which link two computers together in order to handle adequately complex problems. One method, which is in use at Holloman Air Force Base, accomplishes this by using a conventional memory as the communicating link between computers. The basic operation of this type of system is illustrated in Fig. 10. Separate transfer memories A and B serve as links between the two computers. Computer A writes into transfer memory A any data which are needed by Computer B. Computer B may then read these data, process them, and either store the result in its own memory or in transfer memory B from which computer A may then read the data out. This

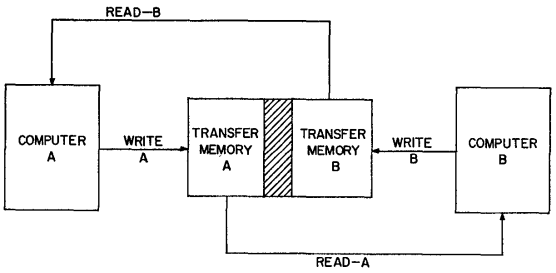

Fig. 10—Two-computer communication link using a transfer memory organization.

two-computer system offers certain advantages in speed over the operation of a single computer.

Another method of linking two computers is being used at the National Bureau of Standards. In this system one computer, called the Secondary, is a slave to the other computer, called the Principal. A similar organization of units within one computer network is used in the IBM 709 computer. Here the Data-Synchronizing Unit is comparable to the Secondary, and the Central Processing Unit is comparable to the Principal. The CPU can assign the DSU an input-output task and then proceed with its own program. The DSU proceeds independently, with the exception of memory access which it must share with the CPU, until it completes its assignment. In this system the program for the DSU is essentially wired in and the memory is time-shared. The National Bureau of Standards system is shown functionally in Fig. 11. The Principal has the authority to assign part of a problem to the Secondary. However, for the Secondary to perform its task it must be supplied with assignment instructions and data. This transfer of data interrupts the operation of the computer *A* memory and thus is time-consuming.

Now consider the advantages of using a "common multiload transfluxor memory" as the communication link between two computers. The functional linkage of such a system is shown in Fig. 12. The common memory is split into three sections to permit the execution of independent writing operations by both computers and any input-output devices. However, the memory is not split for reading, so both computers and other devices can have independent access to any data in the common memory. This common memory will permit three read and three write operations to occur simultaneously.

The significance of this system organization is that the common memory, in addition to acting as a communication link between computers, also serves as the memory-storage unit for each computer. As a result, there is no transfer time involved in communicating between computers. This saving of time is achieved because each computer independently has direct access to any data pertinent to the functioning of the other computer.

Another significant feature of this organization is that the common memory will need less storage capacity than the total amount required by two individual com-

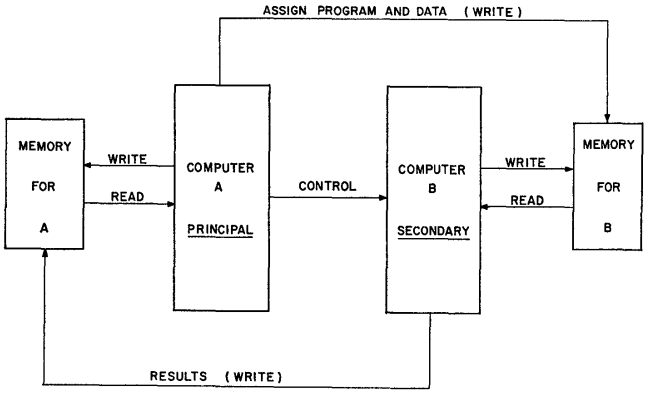

Fig. 11—Two-computer communication link using a Principal-Secondary computer organization.

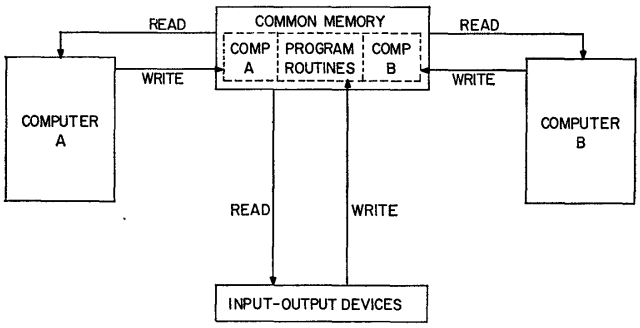

Fig. 12—Two-computer communication link using a common multiload transfluxor memory organization.

puters. This reduction in memory storage capacity can be realized because

1) No transfer memory-storage units are required since each computer has direct access to any data pertinent to the other computer; and
2) Basic subroutines, stored constants, and input data are available to both computers, since both have access to all the memory-storage locations. Thus the duplication of common data is eliminated.

The concept of a master-slave relationship can be carried over to a common memory system but with increased flexibility. The necessity of assigning large blocks of data and several tasks at once to the Secondary in order to keep it operating continuously is practically eliminated. Since all data are directly available to both computers, only the initial address of several stored programs needs to be assigned. In addition the roles of Principal and Secondary can be interchanged at will so that either computer can assign a task to the other.

The system organization as proposed in Fig. 12 requires a four-hole transfluxor memory unit. With a five or more hole transfluxor memory, it is possible to expand this organization to incorporate three or more computers. The more computers in the network, the more efficient the common memory becomes.

Conclusion

The basic mechanisms of transfluxor operation have been shown and a few examples given on how this versatile component may be used.

The multiload transfluxor is constructed by placing additional reading apertures in the core and wiring each hole for separate addressing. This permits many read operations to take place throughout the memory at the same time. Each readout is delivered to its own independent load. The nondestructive read property eliminates the rewrite time associated with conventional core memories; this feature permits cutting the read time in half.

It appears that, by utilizing these properties, considerably more flexibility and speed can be built into a transfluxor memory. The independent operation of the various parts of the memory would facilitate communication between sections of a computer or between two computers and would permit all parts of a computer network to operate without delays due to memory time-sharing. This would be a major advance in computer design.

Design and Analysis of MAD Transfer Circuitry*

D. R. BENNION† AND H. D. CRANE†

I. Introduction

THIS is the second in a series of papers[1] concerned with a technique for performing combinatorial and sequential digital logic with magnetic elements and connecting wires only. These elements are termed MAD's (Multi-Aperture Devices). For clarity, in the first paper the basic techniques were described in terms of simple circuit structures which do not represent the best that can be achieved in the way of operational properties. The object of this paper is: 1) to present circuit techniques for significantly improving the circuit operation; and 2) to present experimental and analytic results which are pertinent to an understanding of the coupling loop operation.

The basic coupling loop and clock cycle are briefly reviewed in the next section.

II. Review of Basic Coupling Loop and Clock Cycle

The circuits discussed here use only POSITIVE MAD elements[1] (although the results are applicable to circuits using other types of MAD elements). Each element has at least two small apertures, one used for an output winding and one for an input winding. The output winding of one element connects with the input winding of another to form a coupling loop, and in this way a pair of electrically connected elements is formed. As information is shifted along a chain of elements, each element alternately plays the role of a receiver and transmitter.

Output Aperture

An element can be in either the Set (binary *one*) or Clear (binary *zero*) state, Fig. 1. Typical ϕ_T-F_T (where F_T is the driving mmf $N_T I_T$) curves for the output aperture of a transmitter for these two states are illustrated in Fig. 1(c). If the element is in the Set state, Fig. 1(b), then flux changes locally about the output aperture in response to small values of mmf F_T, whereas if the element is in the Clear state, Fig. 1(a), flux can change only about a path enclosing both the output and central apertures. Because of the longer, path length in the latter case, larger switching mmfs are required. (Subscript T indicates that this winding is connected with the transmitter end of a coupling loop.)

Input Aperture

A receiver element is always cleared to its *zero* state before transmission into it. It operates then only along a ϕ_R-F_R Clear curve (where F_R is the mmf $N_R I_R$) which is essentially the same as the Clear-state curve for the transmitter, since the relevant path lengths are the same, Fig. 2(a) and 2(b).

An important property of a system in which windings connect with apertures, as indicated here, is that once an element is Set, it is impossible to Clear it from any aperture winding. In Fig. 2(c), an element is shown Set, as a result of current I_R. In Fig. 2(d), the same element is shown after a subsequent "negative set" current, $-I_R$. Note that as a result of the negative set current flux changes only *locally* about the input aperture *without* disturbing the flux about the output aperture.

* This work was carried out at the Stanford Research Inst., Menlo Park, Calif., under the sponsorship of the Burroughs Corp. Res. Center, Paoli, Pa.

† Stanford Res. Inst., Menlo Park, Calif.

[1] H. D. Crane, "A high-speed logic system using magnetic elements and connecting wire only," PROC. IRE, vol. 47, pp. 63–73; January, 1959.