tor as in DCTL. Another very important advantage of the TRL circuit over DCTL is the greater margin afforded by the resistor interstage network against false operation caused by extraneous signals in the ground connections. This improved margin not only implies greater freedom from sporadic errors but also permits greater flexibility in the design of the physical equipment.

Direct comparison has not been made with the other logic circuit configurations, such as nonsaturating current steering circuits, because, in general, systems employing these circuits use more components to meet high-speed objectives, which are not the dominant requirement of the system described. Hence this paper contends that systems employing such circuits are more expensive and perhaps, because of higher component count, are less reliable. Diode logic seems less attractive than TRL because diodes are not competitive with resistors as gating elements, either in terms of cost or in terms of reliability.

Summary

The final chapter on reliability and economics in large-scale data processing systems may not be written for several years. However, the planning and design choices leading toward extensive electronic mechanization are now under way. This paper contends that the logical use of logic devices is leading toward implementation that employs simple circuits. That is, circuit simplicity extracts the best of the past developments on reliable, low-cost components, such as stable d-c power sources and resistors, and couples these with the best of modern semiconductor technology. Such a choice, for the medium-speed data processing system here assumed, is the transistor resistor logic circuit.

A large part of the material presented in this paper represents the work of the writer's colleagues, Mr. E. G. Rupprecht and Mr. Q. W. Simkins. It is hoped that a more extensive and detailed analysis of TRL will be published at a later date.

References

1. Complexity with Reliability, **J. H. Felker.** *Student Quarterly*, Institute of Radio Engineers, New York, N. Y., Sept. 1, 1956.

2. Transistor NOR Circuit Design, **G. H. Royer, W. D. Rowe.** AIEE Transactions, vol. 76, pt. I, July 1957, pp. 263–67.

3. Arithmetic Operations in Digital Computers (book), **R. K. Richards.** D. Van Nostrand Company, Inc., Princeton, N. J., 1955.

4. Transistor Resistor Logic Circuit Analysis, **Q. W. Simkins.** *Proceedings*, Solid State Circuits Conference, Philadelphia, Penna., Feb. 20, 1958. (To be published.)

Direct-Coupled Logic Circuitry

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DIRECT-COUPLED transistor logic circuitry (DCTL), first announced in 1955, has provided many desirable features for digital computer use.[1] Among the principal characteristics of DCTL are extremely simple circuitry, a minimum number of auxiliary components, very low dissipation and power-supply requirements, and the possibility of extraordinary compactness. Various special-purpose machines using DCTL have been built, and at least one class of general-purpose computer has been designed and is in operation. In this paper, the unique features and limitations of DCTL will be considered in detail, together with a brief description of the circuitry and its principles of operation.

Circuit Description

DCTL circuitry takes advantage of the fact that certain types of transistors have useful current gains and impedance ratios with the collector junction slightly forward biased (in saturation), whereas the usual mode of operation calls for a reverse bias on the collector. DCTL operation is unique to transistors; a vacuum-tube equivalent would require useful operation with the control grid more positive than the plate.

Given the possibility of a transistor running with zero or slightly forward collector bias, the basic inverter circuit shown in Fig. 1 becomes possible. This figure shows three cascaded common-emitter inverters, using p-n-p transistors. If the first stage is conducting (in saturation), its collector-to-emitter voltage is sufficiently low that the second stage is held off (nonconducting). With the second transistor not conducting, a sufficiently large current is drawn from the base of the third stage, through the second-stage load resistor, to put the third stage in saturation.

In order to appreciate the possibility of this modus operandi, consider the transistor characteristic curves shown in Fig. 2. These curves are representative of most "wafer" transistors, including alloy-junction, surface-barrier, and similar types, which have negligible series resistance in the emitter and collector leads. On the left of Fig. 2 is shown a set of collector characteristics for the common-emitter connection. These plots of collector current versus collector-to-emitter voltage, with base current the fixed input parameter, show that the transistor maintains good current gain and output impedance with collector voltages of 0.15 volt or less; such curves are representative of both silicon and germanium wafer transistors. The common-emitter input characteristics, shown on the right, indicate that the threshold of significant conduction occurs only with forward biases (negative for p-n-p transistors) greater than 0.1 volt for germanium or 0.6 volt for silicon. Thus it is obvious that the collector-to-emitter voltage of a conducting transistor can be maintained at a lower value than the threshold required for conduction at the input of a succeeding transistor.

Given a DCTL inverter, it is simple to make a flip-flop by connecting two inverters together, as shown in Fig. 3. The mechanism by which the gates affect the flip-flop is as follows: When a gate conducts, its collector-to-emitter voltage becomes low, thus turning off the flip-flop transistor whose base is connected to that gate, in turn causing the other flip-flop transistor (the one whose collector is tied to the gate in conduction) to conduct. Quite obviously, more than one gating circuit could be connected in parallel to either side of the flip-flop, so that the activation of any one or more of the gates on one side would set the flip-flop.

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Many organizations, particularly Philco Corporation, Bell Telephone Laboratories, and Burroughs Corporation, have contributed to the understanding and perfection of direct-coupled transistor logic circuitry. The author is especially grateful to the many colleagues at Philco Corporation and to E. G. Clark and H. J. Tate of Burroughs Corporation, who assisted in the preparation of this paper.

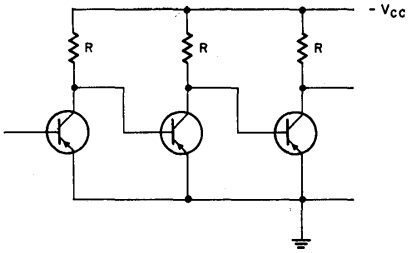

Fig. 1. DCTL inverters

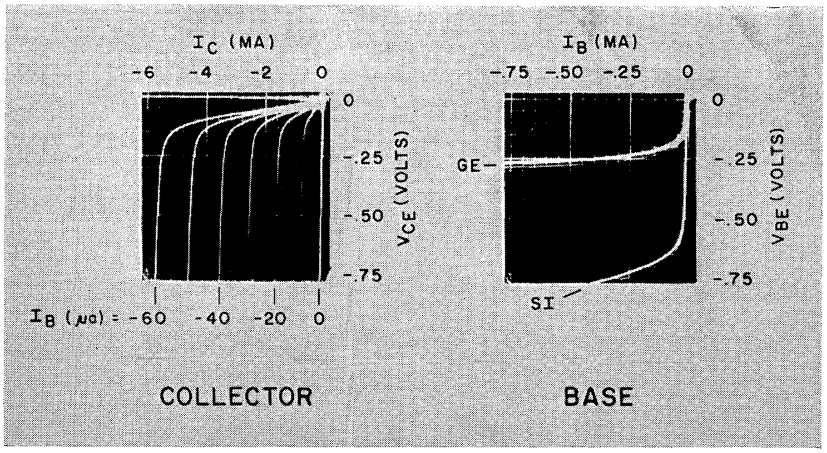

Fig. 2 (right). Transistor common-emitter characteristics

Gating functions can be achieved with transistors either connected in parallel or stacked in series. Examples of parallel and series gates are shown in Figs. 4 and 5. If the transistors are normally in the nonconducting state, the parallel gate could be called an "or" gate, since the output circuit conducts if one or more of the inputs are activated; similarly, the series gate is an "and" gate, since its output conducts only if all the inputs are simultaneously activated. An example of the simultaneous use of both gates to form a half-adder is shown in Fig. 6. The complementary inputs are normally derived from the two sides of flip-flops storing the appropriate input characters. It should be noted that an output signal in the sum or carry channel is the complement of the usually desired signal, in that a "one" corresponds to the low-impedance (conducting), or low-voltage condition. Therefore, it may be necessary in some cases to use an inverter to obtain the appropriate sense for the output signal.

It can be seen that, in general, fewer resistors than transistors are employed in these circuits, and that there is relatively little need for capacitors. One circuit in which a capacitor is required is the one-shot multivibrator, shown in Fig. 7. This circuit is used to generate delays for timing signals, and is triggered by the gating transistor shown in the figure, as suggested by the waveforms sketched there.

Typical practice shows that an over-all system uses roughly 400 resistors per 1,000 transistors and less than 10 capacitors per 1,000 transistors.

Transistor Gain

DCTL imposes a rather severe limitation on the amount of useful gain which can be demanded of each active element. This limited gain results from the need for operating a conducting transistor with low collector-to-emitter voltage. In practice, the number of loads (transistor bases) which can be driven from a single inverter (fan-out) is normally limited to 2 to 3 units in the case of surface-barrier transistors, or perhaps up to six loads in the case of higher gain alloy or microalloy units. The number of gates which can be used to control a single load (fan-in) is somewhat higher, usually set at 1.5 to 2 times the fan-out capability.

In order to understand how these limits are reached, it is desirable to consider the tolerances required for operation of a given interstage. Such an interstage, with n paralleled "or" gates driving m paralleled loads, is shown in Fig. 8. Two conditions are necessary in this interstage. First, when all the gates are off, it is necessary to ensure that all the loads are on. Secondly, it is necessary to guarantee that conduction in any one of the gates will turn off all the loads. The first of these two conditions can be assured by the inequality shown in equation 1.

$$\frac{|V_{CC}(\min) - V_{BE}(\text{on})|}{R_{\text{MAX}}} > nI_C(\text{off}) + mI_B(\text{on}) \qquad (1)$$

In this relationship, the term on the left, the smallest possible load current, is made greater than the leakage current in all the gates plus the minimum required load current in all the loads. The node voltage $V_{BE}(\text{on})$, is a fixed voltage limit, which must appear both in the transistor specifications and the circuit design equations; since it is a limit voltage it requires no tolerances. The second condition is indicated by equation 2,

$$I_C(\text{on}) > \frac{V_{CC}(\max) - V_B(\text{off})}{R_{\min}} \qquad (2)$$

which shows that the collector current of one conducting gate must be greater than the maximum possible current in the load resistor, with the node voltage equal to the specific limit voltage required to maintain the load transistors in the nonconducting state. The important transistor factors required to meet these conditions are as follows:

1. The input impedance of a conducting transistor must not be too low. This fact is assured by setting a maximum limit on "on" base current $[I_B(\text{on})]$ for a particular base voltage, $[V_{BE}(\text{on})]$. This limit is necessary in order to ensure that no one transistor will take too much of the available driving current.

2. The output impedance of a conducting transistor must not be too high. One method of ensuring this condition is to specify that the collector-to-emitter voltage $[V_{CE}(\text{on})]$ be less than a certain maximum value for given collector current and base voltage. An alternative method would be to put a minimum limit on collector current for given base-to-emitter and collector-to-emitter voltages. The ratio of the collector current in either of these alternative tests to the base current in the first test is the minimum transistor gain, which is normally substantially larger than the circuit gain. This ratio, $I_C(\text{on})/I_B(\text{on})$, is usually much smaller than the h_{FE} (current gain) of the transistor in the nonsaturated region ($|V_{CE}|>0.3$ volt).

3. The "off" collector current in a nonconducting transistor must not be too large. This condition is met by putting a maximum limit on collector current $[I_C(\text{off})]$ for a specified base voltage $[V_{BE}(\text{off})]$.

A representative specification for a surface barrier transistor intended for DCTL operation is shown in Table I. The first three quantities in this table ensure that the transistor will function in DCTL circuitry. The last three quantities relate to the high-speed performance of the transistor. Other transistor types have been recommended for use in DCTL operation. The *2N240* surface barrier transistor is specified for switching service, and meets all the requirements for DCTL operation; however, the specification does not guarantee the input impedance. A silicon-alloy transistor, the *2N496*, has also proven satisfactory for DCTL operation, here again, the specified switching

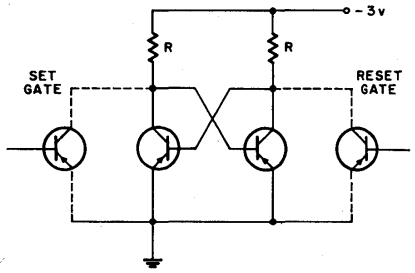

Fig. 3. DCTL flip-flop

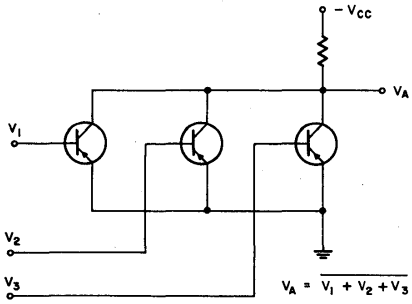

Fig. 4. Parallel (or) gate

characteristics include all the quantities for DCTL operation other than the input impedance.

In order to have compatible connections from one DCTL logical element to another, $V_{CE}(\text{on}) \leqq V_{BE}(\text{off})$. In the case of an "and" gate of two or more transistors, it is necessary to sacrifice gain to reduce the collector-to-emitter voltage, in order that the sum of all these voltages in the series gate will not exceed the "off" base-to-emitter voltage of the loads.

It is possible to relate the transistor gain to component tolerances and circuit gain quite explicity in the case of DCTL. For the single-level interstage shown in Fig. 7, this relation is easily achieved from equations 1 and 2. By solving these two inequalities for the ratio of collector current to base current in conduction, one gets

$$\frac{I_C(\text{on})}{I_B(\text{on})} > m\,\frac{R_{\max}}{R_{\min}} \times \frac{|V_{CC}(\max) - V_B(\text{off})|}{|V_{CC}(\min) - V_B(\text{on})| - nR_{\max}I_C(\text{off})} \qquad (3)$$

This result shows that the transistor gain must be greater than the product of the circuit gain, m, and factors accounting for the tolerances on components. Similar expressions are derivable for more complicated interstages (such as those involving "and" gates). In order to include the effect of component tolerances and "off" leakage current, together with any aging effects in the transistor, it is customary practice to set $I_C(\text{on})/I_B(\text{on}) > 2m$.

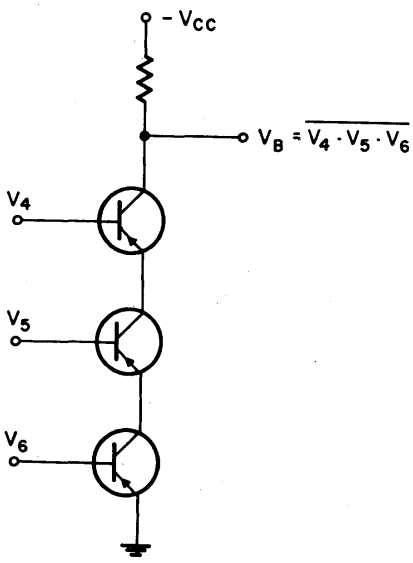

Fig. 5. Series (and) gate

Propagation Time

Two transistor parameters are of principal importance in determining the switching time of DCTL circuitry. First, the transit time, of which the reciprocal of the α-cutoff frequency is a good indication, affects the rise and fall time of a gate. Secondly, hole storage is important, because transistors are driven hard into saturation in DCTL circuitry and show appreciable hole-storage delay time when being turned off.

Switching speed is noticably affected by the extremely low collector voltage at which all the transistors in a DCTL system normally operate, since the α-cutoff frequency decreases with decreasing collector voltage. For a typical surface-barrier transistor, as defined in Table I, gate switching times are of the order of 0.03 to 0.1 microsecond (μsec). Using such transistors in a flip-flop, transition times of the order shown in Fig. 9 are achieved.[2] It is interesting that the switching time decreases with increasing load; this decrease arises because the additional loads reduce the base current, and therefore the degree of saturation, of the flip-flop transitors.

With germanium alloy transistors having 5-volt α-cutoff frequencies of the order of 10 megacycles (mc), switching times of from 0.5 to 2 μsec are experienced. These switching times are generally greater than would be expected, when comparing α-cutoff frequency with the corresponding quantities of surface-barrier transistors, because of the low-voltage operation in DCTL; this fact emphasizes the importance of the effect of low-voltage operation on switching speed.

The switching times observed in DCTL circuits are perhaps 1.5 to 2 times as great as are observed with the same transistors used in conventional resistance-capacitance circuitry having the same gain. However, since higher gains are normally employed with R-C circuitry the speed differential is not as great as 2 to 1. Of course, more refined high-speed circuits, employing nonsaturating or emitter-follower techniques, are appreciably faster, often by a factor of three or more.[2]

Table I. L-5132 Characteristics

$I_B(\text{on})$ <0.4 milliampere, (ma)	(I_C=2.5 ma, V_{BE}=0.293 volt)
$V_{CE}(\text{on})$ <0.075 volt	(I_C=2.5 ma, V_{BE}=0.293 volt)
$I_C(\text{off})$ <85 microamperes	(V_{CE}=−3 volts, V_{BE}=−0.1 volt)
I_{CO} <3.0 microamperes	(V_{CB}=−5 volts)
$f_{\max}$ >30 megacycles.	(V_{CB}=3 volts, I_C=−0.5 ma)
C_c <6.0 micromicrofarads	(V_{CB}=−3 volts)
$r_b'C_c$ <1,500 micromicroseconds	(V_{CE}=−3 volts, I_C=−0.5 ma)

Reliability

There are many factors influencing the reliability of switching circuits. These factors include both internal effects, such as variations in component parameters and in power supplies with age or temperature, and externally generated effects, caused by induced signals (noise) from other circuits or stray fields. Contributing to good reliability in DCTL circuitry are the very-low power dissipation per logical element and the use of a single, uncritical power supply. Mitigating against good reliability are the very-low voltage levels employed within the system and the appreciable dependence on temperature of the "off" current of individual active elements.

Component Tolerances

As suggested by equation 3, it is possible to trade stage gain for component tolerances or for tolerances on supply potential. In general, it has been found desirable to use stable resistors with one-percent tolerances, and design circuits on the basis of at least 3 to 5% variation in component values. With regard to the transistors, in most cases limit (rather than bracket) tolerances are all that is required. For example, if the gain is greater than a certain minimum, or if switching speed is above a certain minimum, no trouble is encountered. The

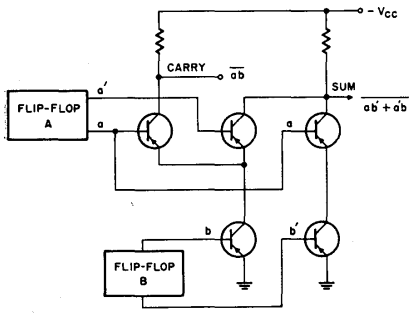

Fig. 6. DCTL half adder

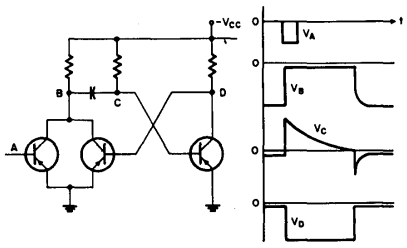

Fig. 7. One-shot multivibrator

one exception is the base-to-emitter "on" voltage for a given degree of conduction. Upper and lower bounds are required here in order to avoid hogging of the available current by one transistor in a multiple load. Fortunately, the input voltage for a given input current in a transistor is not sensitive to aging; in fact, the input current for a given voltage (a more severe condition) does not seem to vary significantly with age. This constancy of input voltage with age is not purely coincidental. It is to be expected that the input impedance in conduction is constant, because it is governed primarily by base spreading resistance (r_b') and emitter saturation current, I_{ES} (not I_{EO}, which includes a time-varying surface leakage current), both of which depend only on geometry and semiconductor resistivity.

DCTL has one particular advantage regarding life which should be noted. The extremely low dissipation in this circuitry subjects the transistors, and resistors, to a minimum of damaging stress from either voltage or temperature rise. Because of this extremely conservative operation, transistors have demonstrated excellent reliability in operating DCTL systems. Experience in various systems has shown failure rates (system malfunction) of less than one failure per 10^7 transistor hours. With such performance, it is possible to design systems with 10,000 transistors and still experience 1,000 hours of useful operation between malfunctions.

Extensive life tests on DCTL transistors have shown that two parameters are mainly responsible for the majority of deterioration with age. First is the "off" leakage current, which tends to increase with time. Secondly, the "on" collector voltage [V_{CE}(on)] for given base and collector currents tends to increase with time (because of the drop in current gain, h_{FE}). Both of these deteriorations are thought to be associated with contamination of the semiconductor surface near the active transistor.

Noise

Some kinds of noise are comparatively unimportant in DCTL whereas others are potentially severe. Because of the very-low impedance level of "on" circuits, capacitive pickup is generally negligible. Power-supply fluctuations are usually unimportant, because voltage translation circuits are not required and the majority of a complete logical system can, if desired, be run from a single supply. On the other hand, because of the small voltage swings which are experienced in DCTL, inductive coupling in either multiconductor cable or via ground leads may be troublesome.

It is generally felt that with germanium transistors a maximum induced noise of the order of 25 millivolts can be tolerated; this figure amounts to 10% of the normally encountered voltage swings

Many alternatives have been suggested for keeping the magnitude of inductive or ground-lead coupling within bounds. In the layout of a single printed-wiring board, it is frequently possible to use separate ground leads for susceptible circuits, or to use wide ground planes for common circuits involving both high-current pulses and susceptible gates. For connections between boards or between parts of a system, various techniques have been evolved. One interesting possibility for this application is the use of load (controlled) circuits which are normally "on" and are turned off by application of an incoming signal; with such operation, a short noise pulse will be ignored by the combination of the low-impedance load and by the hole-storage delay time in the load. A second technique for interplane coupling involves the use of higher voltage swings, and a definite "off" bias, afforded by R-C coupling. Fortunately, either of these techniques adds little complication to an over-all system, because the number of interplane connections can be minimized by designing large printed-wiring boards. In many cases, more than 200 transistors can be mounted on each board, a feat made possible by the small number of auxiliary circuit components.

Finally, contact noise of plug-in connectors is important in DCTL because of the low impedance level that is used in the active circuitry. Here again, large boards with many active elements per board have proven desirable in minimizing this trouble.

Temperature Dependence

Temperature dependence of transistor parameters creates one of the severe limitations of DCTL circuitry. The principal offender is the "off" current, I_C(off), for a fixed base voltage. This current varies exponentially with temperature, as does I_{CO}, and changes by as much as 8% per degree Centigrade, (C). Because of this severe temperature dependence, most DCTL systems using germanium transistors are not designed to operate above 35 to 40 degrees C, although with considerable sacrifice of gain it is probably possible to push this upper temperature limit to 50 degrees C. The upper limit with silicon transistors is in the range of 90 to 125 degrees C. Fortunately, because of the very low power dissipation, modest cooling equipment suffices to keep the system environment within necessary limits in cases where the maximum ambient temperature is excessive.

A second, far less important, effect of temperature is that switching speed tends to decrease with increasing temperature. This decrease is attributable to two phenomena, the increases of r_b' and

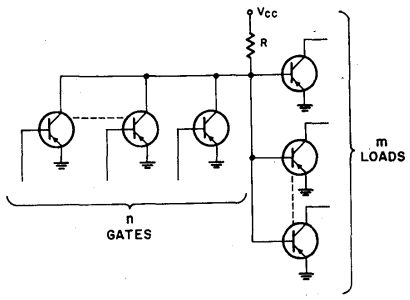

Fig. 8. DCTL interstage

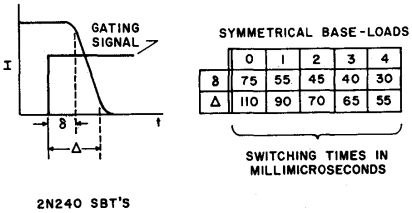

Fig. 9. DCTL flip-flop switching times

of h_{FE} with increasing temperature. The base spreading resistance, r_b', limits the flow of base current during turn-off, while the increase in h_{FE} increases the degree of saturation.

While the upper temperature limit is fairly definite and restrictive, germanium DCTL circuits can be cooled considerably below room temperature without undesirable effect. Although the transistor current gain, h_{FE}, decreases with decreasing temperature, the "off" base voltage, V_B(off), for a given collector current I_C(off), increases; the effects of these two changes tend to compensate each other.

Silicon-transistor DCTL circuitry behaves somewhat differently with temperature than does germanium circuitry, principally because of the lower current gain and higher base voltage of silicon transistors. Because current gain increases with temperature, it is found that silicon DCTL circuitry has wider margins of operation at high temperature than at room temperature. An example of this fact, based on data taken in 1956, is shown in the "schmoo" diagram of Fig. 10. This diagram contains plots of the upper and lower limits of "handle" voltage over which flip-flop operation is achieved.[3] The handle voltage of the DCTL flip-flop is the supply voltage to one side of the flip-flop, with the other side fixed at 3 volts. The particular test circuit on which these data were based employed deliberately selected extreme transistors, one with high gain and one with low gain. It can be seen that the margins of operation are much less critical (broader) at high temperature.

Design Predictability

Most of the important factors in DCTL circuitry are highly predictable, because of the extreme simplicity of the circuit modules. The transistor static parameters are, for the most part, in very close agreement with transistor theory, such as that propounded by Ebers and Moll. The relation between transistor characteristics and circuit performance is also predictable in many cases; an example of this predictability is given by equations 1, 2, and 3.

The prediction of switching times is again relatively simple, except for the fact that transistor parameters such as the α-cutoff frequency vary rapidly with operating point near the saturation region.

The two areas in static design where predictability is difficult are the stacked "and" gates and circuits operating at rather high currents. In the latter case, transistor nonlinearities become appreciable. This nonlinear region may begin at current levels as low as a few milliamperes for some extremely small transistors, particularly surface-barrier types.

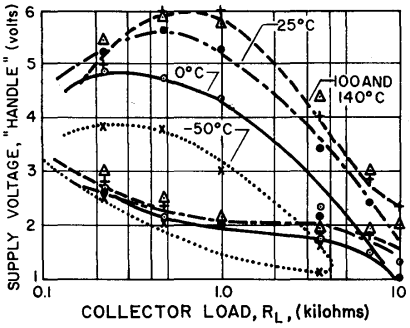

Fig. 10. Operational boundary (schmoo) diagram of silicon DCTL flip-flop

Marginal Testing

The possibilities for good marginal testing procedures are limited with DCTL, because there is generally only one power-supply potential. The usual procedure has been to split this supply into two sections, one supplying each side of all the flip-flops in the logical circuitry. The disadvantage of this procedure is that it renders the circuits somewhat more susceptible to power supply noise, since differentials can exist in the voltages supplied to the two halves of a flip-flop. Nevertheless, since there is little else that can conveniently be varied, this technique is still being employed for marginal checking.

Physical Properties

DCTL probably represents close to the ultimate of circuit simplicity and minimization, within the bounds of presently available diode or triode logical elements. (Such complex logical elements as the 4-terminal full adder recently described by R. F. Rutz[5] will no doubt make for even greater circuit simplicity at such times as they become producibly practical.) In general, only one class of transistor and one or two values of resistor are required for a complete logical system. Because of the small total number of components, the number of interconnecting nodes is likewise kept to a minimum.

The over-all cost of a DCTL system is very comparable with that of an equivalent system employing alternative circuit techniques, at least in the case of special-purpose computers. Admittedly, the cost per component is high, because most of the components are transistors and not inexpensive resistors, and because the transistors have to meet fairly stringent specifications regarding low-voltage current gain and impedances. However, because of the circuit simplicity and ease of design, engineering and assembly labor is minimized. Therefore, even though the component cost is high, the over-all cost in the manufacture of a limited number of special-purpose machines is fully competitive with that of a comparable design using alternative circuitry. One might say that DCTL eliminates a large fraction of the nodes of a logic system in exchange for a comparatively large number of fairly tight transistor specifications.

The logical design of a DCTL system is very close to the final electrical layout, because each logical element is normally equivalent to a very simple combination of transistors and at most two resistors. In fact, DCTL circuitry is very much like relay logic circuitry, with the exception that the individual elements are single-pole, single-throw switches with an interconnection between input and output circuits. Nevertheless, within the framework of specific rules of logical design, which are more restricted than in the case of relays, the conversion from design to finished hardware is very straightforward.

System Features

DCTL systems are probably more adaptable to compact packaging than any other competitive system, because of the small number of components and the lower power consumption of this circuitry. Although the circuitry demands rigid transistor requirements, it treats the transistors gently, so as to minimize the rate of aging. Probably the principal areas in which DCTL systems are presently applicable are those in which space and power consumption are at a premium.

The application of this class of circuitry will be greatly extended when economically competitive silicon transistors become available, both because of the higher maximum temperature and, more particularly, the easing of logical design rules made possible by the higher base-to-emitter potential in conducting silicon transistors. Various transistor types have already been specified for DCTL, thus eliminating any problem of component availability.

Summary

Direct-coupled transistor logic circuits are distinguished from conventional

switching circuits by a substantially smaller number of components and connections, and by extremely-low power consumption. Circuit simplicity and low dissipation are obtained at the price of limited gain, small voltage swings, and a comparatively low upper limit on internal temperature. Rather severe requirements on transistor parameters, particularly input impedance and saturation voltage, are compensated by almost negligible dissipation and maximum voltage requirements. The total cost using DCTL is comparable with other techniques, because the tightly specified transistor eliminates considerable complexity in system design and manufacture.

References

1. Surface-Barrier Transistor Switching Circuits, **R. H. Beter, W. E. Bradley, R. B. Brown, M. Rubinoff.** *Convention Record,* Institute of Radio Engineers, New York, N. Y., pt. IV, 1955, p. 139.

2. High Speed Transistor Computer Circuits, **S. Y. Wong, A. K. Rapp.** *IRE-AIEE Transistor Circuits Conference,* Phila., Pa., Feb. 1956. (Not published.)

3. High-Temperature Silicon-Transistor Computer Circuits, **James B. Angell.** Proceedings of the Eastern Joint Computer Conference, *AIEE Special Publication T-92,* Dec. 10–12, 1956, pp. 54–57.

4. Large-Signal Behavior of Junction Transistors, **J. J. Ebers, J. L. Moll.** *Proceedings,* Institute of Radio Engineers, New York, N. Y., vol. 42, Dec. 1954, pp. 1761–72.

5. Two-Collector Transistor for Binary Full Adder, **R. F. Rutz.** *IBM Journal of Research and Development,* New York, N. Y., vol. 1, July 1957, pp. 212–22.

Symmetrical Transistor Logic

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THIS paper discusses symmetrical transistor switching circuit techniques. The circuitry is designated "symmetrical circuits" because the basic circuits employ both p-n-p and n-p-n transistors in approximately equal numbers which result in networks that exhibit a high degree of operational and topological symmetry. The major practical advantage of this circuitry over other types lies in the ease with which basic circuits may be integrated into a digital system. This advantage is made possible through, 1, keeping the circuit configurations flexible (to satisfy many different system applications), 2, worst-case circuit design with regard to component stability and system loading requirements, 3, use of only standard commercially available components, and 4, insisting that all present-day circuit designs be applicable to known future device trends. The major criticism of the symmetrical circuit techniques is that the circuits require a greater number of components for a specific equipment than do other types of circuitry that can be engineered to build the specific system. However, it is felt that this criticism is not justified in this case for two reasons. They are: 1, The additional cost of components required for symmetrical logic is more than counterbalanced by the shorter system realization time required. This is particularly true for an establishment, such as the Massachusetts Institute of Technology Lincoln Laboratory, that is engaged in system research and development. And, 2, that symmetrical logic techniques are more adaptable to future developments in the device, circuits and system area than other types of circuit logic.

It is the purpose of this paper to show why, when, and under what conditions symmetrical circuit techniques should be used, along with probable future developments, through the discussion of the circuit techniques and relating their circuit capabilities to the solution of system problems.

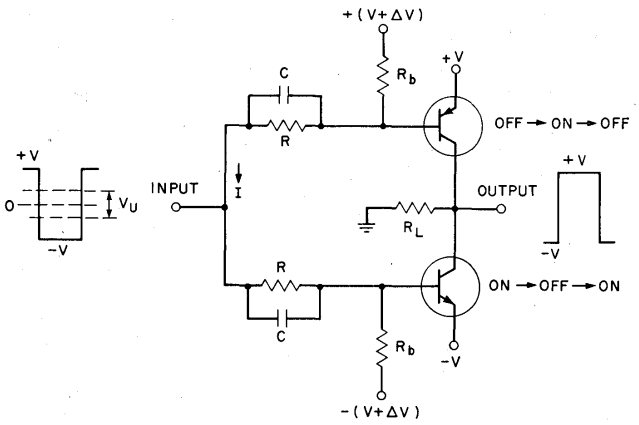

Fig. 1 (right). Symmetrical buffer inverter

I. Basic System Requirements

A. Initial

The initial specific system for which the symmetrical circuit approach was intended had the following requirements:

1. General-purpose computer applicable to real time problem solution.
2. All solid-state machine.
3. Nonairconditioned ground environment.
4. Synchronous machine with a basic clock rate of 3 microseconds, (μs).
5. Memory capacity of 8,192 registers, 28 bits in length, with a memory cycle time of 6 μs.
6. Semiportable housing.
7. Minimum conception to completion time with a minimum of staff.
8. Maximum reliability with minimum maintenance.

B. Additional

It was also the goal of the circuit designer to build circuitry that was sufficiently flexible to meet requirements for all other ground-based digital-data processing systems contemplated at the time (there were several).

II. Basic Circuit Modules

A. General Comments

Aside from the general system requirements of Section I, there are several other component-circuit-system requirements worthy of special note. They are:

1. That the circuits require minimum-specification components (single-ended specifications when possible).
2. That all components be commercially available stock items.
3. That the circuit techniques be sufficiently flexible to incorporate future higher performance devices to satisfy future

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