However, there are still two good spares available, so that three repair technicians plus $8+(3-2)=9$ amplifiers will be required.

It may be questioned as to whether such extreme confidence levels are required. In each case, the physical nature of the problem at hand should be examined carefully, and analytical results used as the best guide to determine appropriate parameters. It is interesting to note that we cannot replace spares by technicians directly, but must consider the factors involved. Doubling or tripling the number of technicians will not reduce the number of spares required in the same proportion.

The part played by the delay in the pipe line shows up very noticeably. To minimize these losses, as short a pipe line delay as possible should be the aim of the logistics pattern.

These few aspects of the base-field station example merely indicate one approach in which spares estimates can be used for setting up logistics procedures. More detailed analyses can be carried out for complete solution of some logistics system problems. It can be recognized that determination of a logistics scheme is similar to that of inventory control, and is another aspect of the more general waiting-line problem.

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Accuracy Control Systems for Magnetic-Core Memories

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Introduction

WHY BE concerned with means for improving reliability in magnetic-core memories? The coincident-current magnetic-core memory has proven to be the most reliable medium yet devised for high-speed storage in digital computers. Experience with core storage at BIZMAC, as well as at Lincoln Laboratory and at RAND,[1] shows that one can achieve mean times between errors measured in the hundreds of hours. Should this, however, be the basis for complacency? Such performance, although an order of magnitude better than has been reported[2] for electrostatic storage, is only comparable to those of the arithmetic and control portions of the computer.

It is our basic premise that core memory performance, while presently adequate, will not long suffice in view of the trend toward greater complexity resulting from increases in memory speeds and capacities. If this premise be accepted, then it follows that means must be provided for enhancing memory reliability. Two such means will shortly be described.

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[1] RAND JOHNNIAC. See *Digital Comp. Newsletter*, vol. 8, April, 1956.

[2] J. M. Wier, "Reliability and characteristics of the Illiac electrostatic memory," *Proc. East. Joint Comp. Conf.*, pp. 72–77; 1953.

Accuracy Control

Reliability has been defined "as the probability of a device performing its purpose adequately for the period of time intended, under the operating conditions encountered."[3] In the case of a computer, a transient fault can invalidate the results of extensive computation. A useful measure of system reliability is, then, the probability of error-free operation during a given run as a function of the duration of that run.

The usefulness of the processed results is directly related to system reliability. In executing its instructions, the computer must accurately perform the many transfers and transformations whereby data is processed. Control of accuracy is facilitated by checking: programmed, built-in, or some combination thereof. The importance of checking and the extent to which it is applied depends on the consequences of improper operation. If these consequences are measurable, then the "best" combination may be determined on an economic basis. More frequently, however, the balance is established empirically, and consequently reflects the wide variance of opinion as to the "best" combination.

[3] L. M. Clement, "Reliability of military electronic equipment," *J. Brit. IRE*, vol. 16, pp. 488–495; September, 1956.

Magnetic-Core Memories

In the course of the past two decades there have been several generations of memory devices. Although many devices are capable of retaining binary information, relatively few lend themselves to rapid selection. One of these few, the bi-remanent magnetic core, has recently become the "standard" storage medium in high-speed computers. The individual core acts as an elementary cell capable of storing one binary digit. As shown in Fig. 1, the core stores a "0" when in positive remanence; "1," in negative remanence. The memory element is relatively insensitive to an applied field H_d, but is responsive to a field H_m resulting from the coincident application of two fields of value H_d. By virtue of this nonlinearity, the cores provide an added degree of discrimination which greatly simplifies the selection problem.

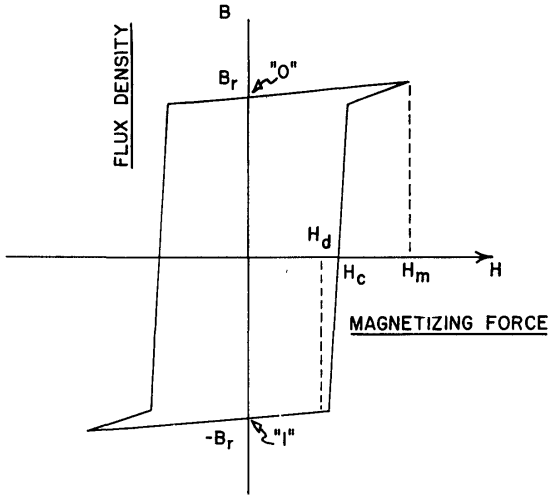

Fig. 1—Hysteresis characteristic of memory core.

Coincident-Current Operation[4–6]

The principle of operation will briefly be reviewed. In the array shown in Fig. 2, each core is threaded by four windings: the sense and the inhibit windings are common to all cores, a particular x coordinate and a y coordinate access line threads each core. The content of a specific core is read by applying a drive current I_d along each of the appropriate access line pair. Only the core at the intersection is driven by $I_m = 2I_d$, and only that core responds. If it contains a "1," a relatively large voltage is induced in the sense winding; if a "0," a relatively small voltage. In Fig. 2, the content of core 21 is being read by driving lines X_2 and Y_1.

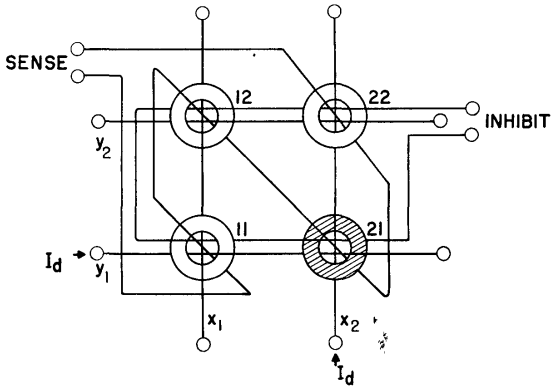

Fig. 2—Planar array of memory cores.

To write information into a core, the drive currents are reversed. If a "0" is to be inscribed, a bias current having magnitude I_d and sense opposite to the drive current is applied to the inhibit winding; if a "1," no excitation is applied. Note that the extraction of the content of a core results in destruction of the information in that core—whatever its original content, it will be "0" after reading. Hence, an access to the memory requires a "read-write" cycle if the information must be preserved for later use.

The planar arrays are arranged to form a compact, three-dimensional lattice by interconnecting corresponding x lines and y lines. Each array serves as a digit plane since it stores a particular digit for each of the registers in the lattice. Storage elements are selected by suitably controlling the currents in the three coordinates along the edges of the lattice. Since the selection coordinates are entirely spatial, the rate of access to any register is inherently high.

A block diagram of the basic memory configuration is shown in Fig. 3. A particular core register is selected by the X access and Y access means. Each of these consists of an address register, selection matrix, access drivers, and access switches. The information channel includes digit drivers, sensing amplifiers, strobe gates, pulse standardizers, a memory register, and a network for gating information to and from the memory. There is also a memory-timing generator which converts the basic machine commands into pulses of a nature determined by the characteristics of the cores.

Accuracy-Control Means

Having reviewed the basic ideas, let us now consider two systems for the detection and location of memory faults. The first of these determines if the desired register has been selected; the second, that the desired information has been inserted into the memory. In each case, the actual results are monitored and compared with the results desired. If the comparison fails, an alarm condition is indicated and the machine is stopped.

[4] J. W. Forrester, "Digital information storage in three dimensions using magnetic cores," *J. Appl. Phys.*, vol. 22, pp. 44–48; January, 1951.
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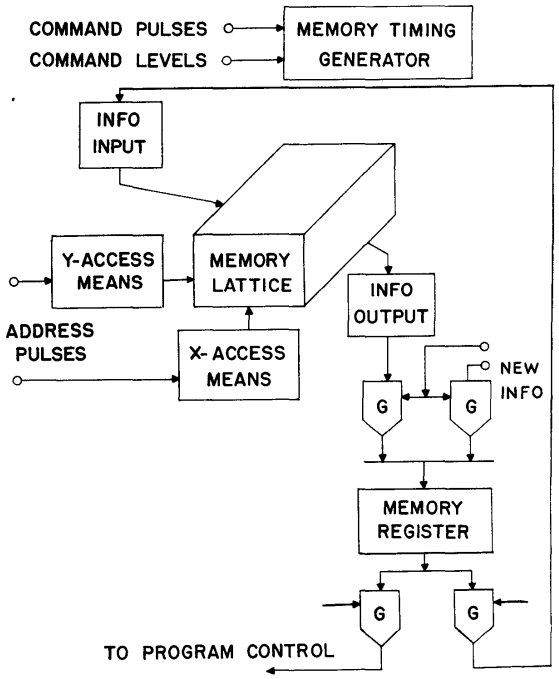

Fig. 3—Block diagram of core memory.

Checking of Register Selection

The block diagram of the core memory has been redrawn in Fig. 4 to show those areas pertinent to the selection of a core register. With each access system is now associated a magnetic-core error matrix, the outputs of which are fed to a logical network which determines if an alarm condition exists. The details of a check system for one access dimension (8 lines) are shown in Fig. 5.

The theory of operation is as follows: in the course of a memory cycle, the binary code for the desired line is set into the memory address register from a counter in the program-control portion of the computer. A coordinate line, hopefully the correct one, is then driven by one of the access drivers. Each line threads its way through the memory lattice, and then through the appropriate set of error cores (represented by the short diagonal lines) with six turns. Thus, if a current of value I_d produces a magnetizing force H_d in the memory cores, it will produce $6H_d$ in the error cores. Since the error cores are identical in characteristic with the memory cores, the appropriate set of error cores will be switched whenever a line is driven.

Examination of the error matrix shows it consists of two parts: the leftmost two columns of cores determine the parity of the line being addressed, while the rightmost three columns re-encode from linear to binary. The outputs of the parity-detecting cores are amplified and fed to a network which checks that at least one and no more than one line was driven during the memory cycle. The outputs of the address-encoding cores are also amplified and fed to a network where the address code

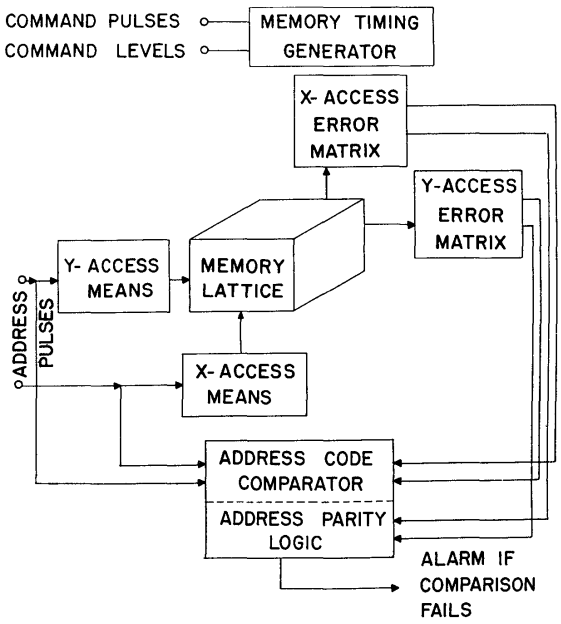

Fig. 4—Checking of register selection.

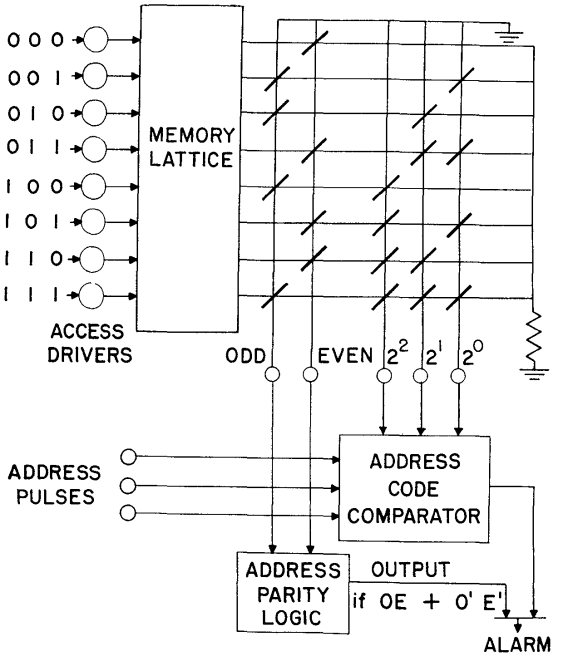

Fig. 5—Error-matrix and comparison logic for one access dimension.

sent by the originating counter is compared against that of the line driven. An alarm is indicated in case of malfunction.

The system just described will detect and locate faults which occur in register selection. Since the current in the access line is monitored, no link in the selection chain is permitted to function without scrutiny. The control loop is closed around the entire selection system.

If economy, space, or weight are the overriding considerations, then a simpler checking system might be

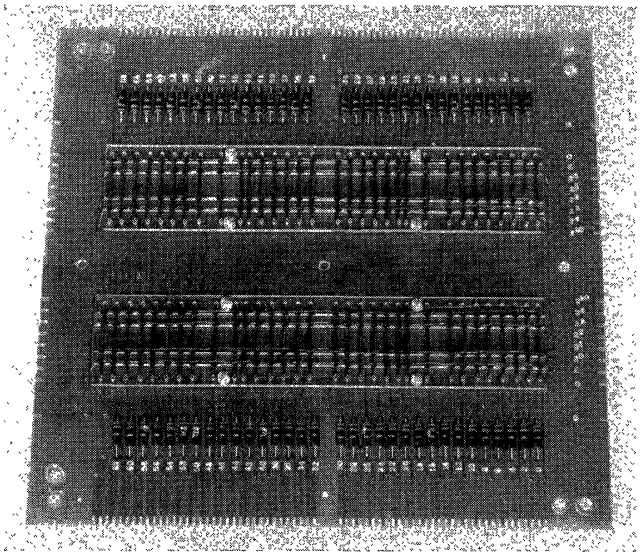

Fig. 6—Error matrix.

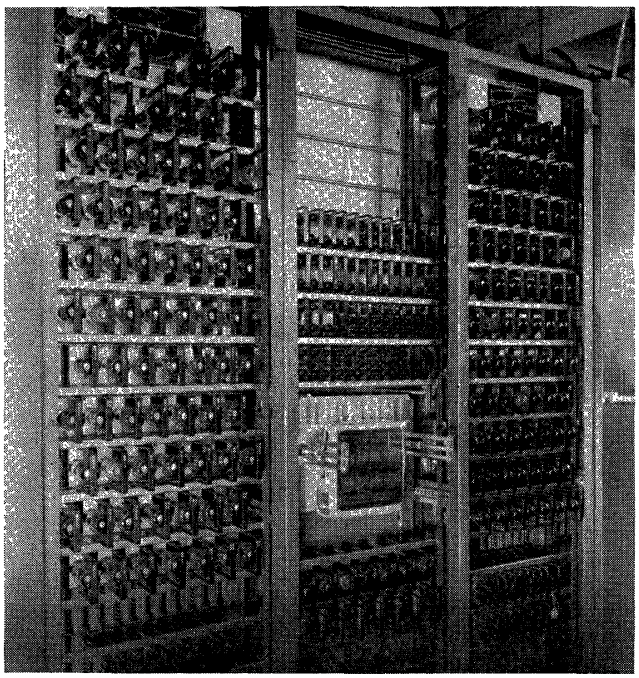

Fig. 7—Error matrix under test.

based on the parity-detecting cores. This system would detect single faults, but would be of less effectiveness in locating the fault.

A photograph of the error core matrix is shown in Fig. 6. Note that the design is such that it may readily be assembled with the memory arrays into a complete lattice. A photograph of the prototype error matrix under test is shown in Fig. 7. Fig. 8 shows a photograph of the error-core outputs from the sensing windings when the matrix is in operation. Condition I shows the outputs of the parity-detecting cores under proper addressing, which is addressing one line at a time. Condition II shows one form of improper addressing, which is addressing two lines simultaneously caused by an open diode in the address matrix.

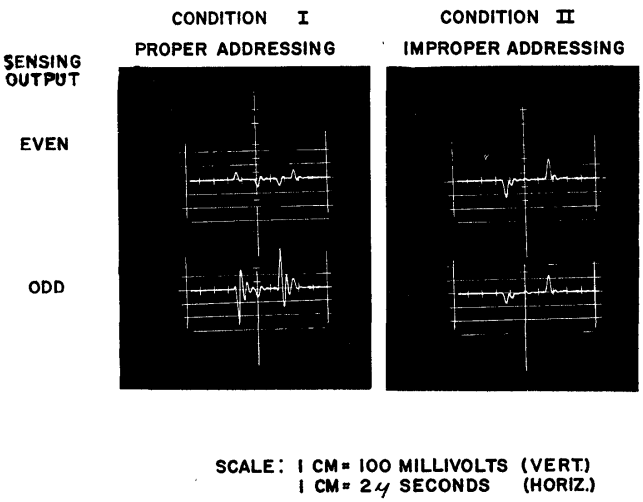

Fig. 8—Error-core outputs.

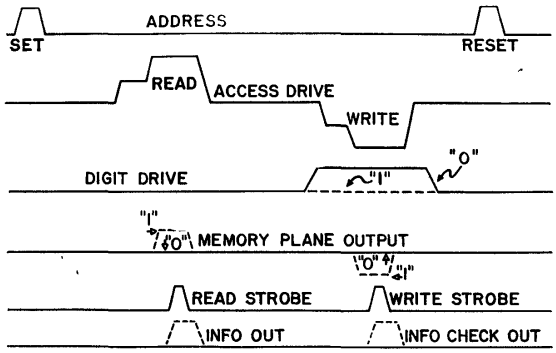

Fig. 9—Memory-timing diagram.

Checking of Information Insertion

Control of this memory function is extremely simple in concept. We recall that this memory operates on the principle of a "destructive read-out." Hence each memory access is characterized by a "read-write" cycle. If one examines the timing diagram shown in Fig. 9, one finds that an output is produced from each core in the selected register during both the "read" and the "write" portions of a memory cycle. For either portion, a relatively large output indicates storage of a "1"; a small output, a "0." Whereas the output at "read" time identifies the information which had been stored during an earlier memory cycle, that at "write" time identifies that just inserted in the core. By providing an additional strobe pulse, the core output at "write" time may be sampled and stored in a memory check register.

Referring to Fig. 10, one finds a simplified diagram showing the information channels with their associated accuracy-control logic. Since the memory register contains the information that should have been stored in the core register, and the check register that which actually was stored, a comparison can be made. In case of error, an alarm is indicated and the machine is stopped. Here again the control loop is closed around the entire function, since it is the final remanent state of the memory core that is being monitored.

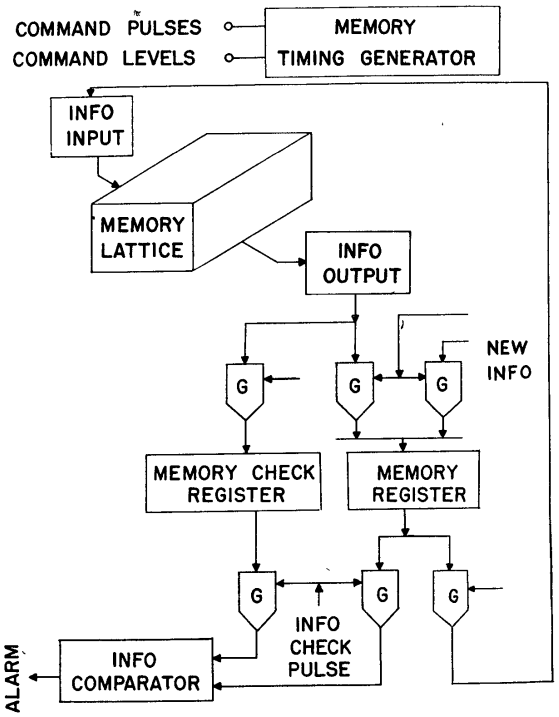

Fig. 10—Checking of information insertion.

Balance In Means for Checking

The provision of checking features, be they programmed or built-in, requires additional apparatus, increased machine working time, or both. These consequences must be weighed against those resulting from improper operation of the system. Furthermore, a balance must be struck between the relative proportions of programmed and built-in checking. The more built-in checking provided, the higher will be the initial cost. A hardware-checked machine, however, will provide savings in operation through reductions in the following:

1) programming costs,
2) program debugging costs,
3) key-punching costs,
4) computer running time per task,
5) storage requirements.

Where clearly desirable, hardware checks should be provided in a manner consistent with the system philosophy and with the needs of the particular application. The amount of additional apparatus required may be held to a minimum by designing around checking features inherent in the system and by integrating all such features on a system basis.

It should be noted that no amount of checking will, of itself, produce useful data. Implicit throughout has been the assumption that the computing system is the end product of mature circuit and system design, and of high standards of workmanship.

Conclusion

The importance of checking computer operations is generally accepted. Economic considerations stemming from consequences of improper operation dictate extent and means for implementing checks. A balanced combination of built-in and programmed checking appears to be adequate for commercial applications.

Two systems are discussed for improving the reliability of operation of a magnetic memory. These systems, simple in concept and economic in implementation, provide checking functions which are extremely difficult to accomplish by programmed means. By detecting and locating faults as they occur, these checking systems will raise the general level of performance of the memory. Improvement in performance is necessary if we are to keep pace with the continuing trend to higher capacity and speed in computer memories.

Discussion

E. J. Otis (Daystrom Systems): In Fig. 5, if lines such as 7 (111) is selected, and line 2 (010) is by mistake pulsed, how is the system going to recognize the error?

Dr. Katz: Line 7 consists of three ones, and line 5—line 2 (010) are both of odd parity, so that the parity detecting cores would not sense this error. However, the address and coding cores would encode 111, which is the proper address. From this we go right into the address code-comparator, and compare favorably with the address pulse. The parity-detecting cores, which I mentioned earlier, would not detect the error. This error, however, involves the failure of two bits; in other words the two to the zero, and the two to the second bit have failed, and such a simultaneous failure is very unlikely, but this would not have detected it. Now I should amplify it by saying that this system will detect all single-bit failures; seven out of eight 3-bit failures, etc. I did mention that although this system would detect virtually all errors, it will not detect this particular error.

John Paivinen (General Electric): Please repeat the description of how data check is performed. Is it read-out following a write operation, or are the inhibit drivers monitored?

Dr. Katz: Neither, actually. In the process of writing information into the core, if the core were to receive a one, it would be switched and go back to $-B_r$ in this region. If it were to have a zero inscribed, it would not switch and would be a relatively small output. The same sense findings would see both outputs, C_1 and read times, as well as C_1 and write time. And the same sense amplifier would amplify the signals, since the response is both positive and negative polarity signals. By providing an additional strobe, at a different time, one can examine the output of the plane at the time of writing. The same sensitive equipment that is involved in normal reading is again used in checking. We do not monitor the current in the inhibit drive.

Vaughn Winkler (IBM): You indicated 15–30 per cent more equipment was required for register selection. How much additional time was required for information channe checking?

Dr. Katz: That 15–30 per cent was pulled out of context. The 15–30 per cent check applies to the total system, in that it means an increase in equipment for the total system. Now, the two systems described here—the increase and the equipment associated with the computer—as far as these two checks were concerned, would only be about 5 to 10 per cent of the memory itself. It would increase the digits for the most elaborate address check, and the information check. Now the information check is a function of how many bits are in a word; and the address check depends on how many bits determine one dimensional of access.

Now insofar as additional time on the information, there is no additional time on the register selection check; this happens in the process of reading. With respect to the information check, there is possibly another half-microsecond cycle, which is a staggering of the write pulse, resulting in less noise at the write time. The strobe occurs at the write time.