of the $B$-$H$ loop in about 16 joules per cubic meter. The loss can be further compared with that of a ferroelectric condenser made of BaTiO$_3$ with $E_c = 600$ volts per centimeter, $50,000$ volts per meter, and $D_r = 0.18$ coulombs per square meter. The area of two quadrants of the $D$-$E$ loop is about 18,000 joules per cubic meter.

Conclusion

Experimental results indicate a straight-line relationship between reciprocal switching time and applied magnetic field for superconductors. The fastest switching observed to date at Massachusetts Institute of Technology is 0.1 microsecond for a thin-film cryotron. Switching energy density is approximately 2.5 joules per cubic meter as contrasted to about 8 for ferrites and 9,000 for ferroelectric barium titanate.

References


Discussion

J. L. Nevins (Massachusetts Institute of Technology Instrument Laboratory): What is the present switching time for cryotron elements?

Mr. Slade: Dudley Buck has reported switching a single film cryotron in 0.1 microseconds and there have been unofficial reports of faster switching times. However, the control coil of a cryotron is entirely inductive, and if it is being driven by the gate of another cryotron, as it often is, the switching time of the circuit is much longer. The time constant of such a circuit is governed by the coil inductance divided by the gate resistance. For present-day cryotrons this switching time is about 500 microseconds.

H. Robbins (Hughes Aircraft): How many watts of refrigerator power are needed for each watt of power dissipated in the cryotrons?

Mr. Slade: A theoretically perfect refrigeration machine would require a ratio of input power to dissipated power approximately equal to the ratio of room temperature to 4 degrees absolute: or about 100 to 1. Because of the inefficiency of the machine I would estimate that for an actual machine the ratio is about 600 watts input power for every watt dissipated. This is not as serious as it might seem because cryotrons dissipate so little power. For instance, in a particular cryotron memory system, reported in this issue, no power is dissipated under steady state conditions, and the memory dissipates only 5 microwatts during a normal interrogation.

R. J. Schubert (Westinghouse Electric Corporation): What are the limits of switching time (transition periods) in view of the penetration depth with respect to the dimensions of the superconductor?

Mr. Slade: Switching of superconductors has not been observed in times shorter than $10^{-8}$ seconds because of instrumentation difficulties. The low magnetic-field strength steady-state behavior of superconductors as measured by the Q of a resonant superconductive cavity show that superconductors start to show small amounts of resistance in the 3,000 megacycle region. In the infrared region materials do not exhibit superconductivity at all. Therefore, one may infer that there is a relaxation spectrum for superconductivity which falls off somewhere in the short microwaves. Recent measurements at the Westinghouse Research Laboratory in East Pittsburgh, Pa., verify this. It is not possible to conclude at what upper frequency superconductors can be switched, but if the high magnetic-field strength and low magnetic-field strength characteristics drop off at the same frequency then the shortest switching time may be in the $10^{-8}$ region.

R. Jepperson (International Business Machines Corp.): Are not difficulties encountered in connecting inputs and outputs, since a wire passing from room temperature to operating temperature would have many conducting states?

Mr. Slade: No, there are no difficulties in this respect. Zero-resistance interconnecting wires are of course desirable in order to minimize joule heating, but they are not necessary. The resistance of the input and output leads merely adds to the resistance of the external equipment. Superconducting wires are only necessary within a logical building block such as a flip-flop or a multi-position switch.

A 2.5-Megacycle Ferractor Accumulator

R. D. TORREY  T. H. BONN

Investigations of magnetic amplifiers at high frequencies indicate that reliable operation with a power gain of about three or four is possible at an information frequency of 2.5 megacycles using series pulse-type magnetic amplifiers. A unit employing several cores was constructed in order to gain experience in packaging and with operating problems at this frequency. Before going into a description of the unit itself a short explanation of the operation of the magnetic cores is given.

The clock- or power-pulse source for the cores is a low impedance 2.5-megacycle sine-wave source with a peak amplitude of 20 volts. A tapped output transformer is used supplying two phases of clock power 180 degrees apart at both full- and half-amplitude voltages.

At this frequency a sine-wave clock offers advantages over square wave or other discontinuous types of clock wave forms. Several of these advantages are

1. Ease of generation and distribution. Generation of sine-wave power at high frequencies offers no problems. The requirement of a low source impedance means a distribution system with high distributed capacity, and a sine-wave clock supply that allows this capacity to be tuned out.

2. Reduction of diode-enhancement effects. Measurements of effective reverse leakage have been made on rapid-recovery type diodes at 2.5 megacycles. These measurements indicate that the effective reverse leakage using a sine wave is about one half the leakage expected using a square-wave clock. The reduction in leakage results from the fact that diode currents are decreasing toward the end of the cycle.

3. The losses due to core winding and wiring inductances are minimized when using sine waves. These losses appear as a phase shift of output, with most of the energy...
stored in the inductors being regained toward the end of the cycle. This advantage is not realized if diode-resistor constant-current gating networks are used between cores, for then the core loads may appear as constant-current sinks. In this case the energy stored in the inductors is returned to the clock source rather than to the loads.

The magnetic amplifiers used are of two types, an amplifier which gives an output on receipt of a signal, and an inverting or complementing type amplifier which gives an output only when no input signal is present. These two types of amplifiers are all that are necessary to perform all logical functions.

The amplifiers are series pulse type amplifiers, with a cycle of operation divided into an input period and an output period. Thus, there is a pulse time delay of 0.2 microsecond in going through each amplifier. A diagram of the complementing or inverting type amplifier is shown in Fig. 1.

The core itself consists of five wraps of 1/8-inch wide, 1/8-mil thick, 4-79 Permalloy wound on a 0.1-inch diameter stainless steel bobbin. Input and output windings of no. 43 high-frequency wire are applied as shown. Operation of the circuit is as follows:

At the end of a power pulse the core is left in a state of positive saturation. As the power pulse at terminal nine goes negative, resistor \( R_1 \) will clamp in at +3 volts through diode \( D_5 \). The lower end of \( R_1 \) will be clamped at ground potential through the input diodes and diode \( D_4 \) of the previous stages.

In the absence of an input pulse during the time the power pulse is negative, a current will flow from the 3 volt blocking source through the input winding and resistor \( R_3 \) to the now negative clock line. This current will overcome any reverse leakage through the output diode \( D_4 \) and maintain the core at positive saturation. The core is then a low impedance to the following positive clock pulse and a large output will result.

If, however, an input pulse is present as the clock goes negative, the input terminal four will be raised above 3 volts, and a current will flow from the input terminal through the input winding and resistor \( R_4 \) to the now negative clock line. This current is in a direction to switch the core from positive to negative saturation. When at negative saturation, the core will present a large impedance to the following positive clock pulse as it switches from negative to positive saturation, and only a small magnetizing current will flow in the output winding as the core switches from negative to positive saturation.

A positive blocking pulse of half the power-pulse voltage is applied to the output circuit through diode \( D_4 \) during the time the power pulse is negative. This insures that there is sufficient back voltage across diode \( D_4 \) to keep it open while an input signal is switching the core from positive to negative saturation.

The input circuit of the core is disconnected during its power-pulse period since the whole input winding is raised by the positive power pulse, opening the input diodes and diode \( D_4 \). Therefore, the presence of the blocking pulse from other cores on the input line during this time has no effect on the circuit.

In the absence of an input pulse, a current will flow from the 3 volt blocking source through the input winding and the resistor \( R_3 \) to the now negative clock line. This current in a direction to reset the core from positive to negative saturation. When at negative saturation the core presents a large impedance to the following positive clock pulse as the clock pulse switches the core from negative to positive saturation. During this time
only a small magnetizing current flows in the output circuit, and this current is absorbed by the combination of resistor $R_3$ and diode $D_3$, yielding no output pulse.

If, however, an input pulse is present during the time the power pulse goes negative, the input terminal will be raised in potential above the reverting pulse, and a current will flow from the input terminal through the input winding and resistor $R_2$ to the negative clock line. This current is in the direction to hold the core at positive saturation, and to overcome any reverse leakage through diode $D_2$ tending to reset the core to negative saturation.

The same output blocking-pulse considerations apply to the amplifier as well as the complementer, for when the reverting pulse switches the core from positive to negative saturation a voltage will be induced in the output winding to cause diode $D_2$ to conduct and load the input winding. In this amplifier the same waveform is used for reverting the core and blocking the output winding.

The numbered terminals appearing on the figure refer to the pin numbers of the novel header in which the core is mounted. Because of the small physical size of the components, a core and all associated resistors and diodes can be mounted in a small sealed header, yielding a completely self-contained logical package. Input diodes are also mounted in clusters in a header.

The clock transformer is illustrated in Fig. 4. It is of special construction to 

The clock transformer is illustrated in Fig. 4. It is of special construction to minimize leakage inductance. The primary winding is of single-layer center-tapped construction, and the output winding consists of a thin, flat strip with the same over-all width as the primary. This type of construction yields a transformer with an output-winding leakage inductance of approximately 5 milli-microhenries.

The radio-frequency transmission line is effectively an extension of the transformer output winding, and consists of five strips of 4-mil copper tape separated by layers of 2.5-mil insulation. The inductance of the transmission line between adjacent conductors is approximately 0.4 milli-microhenries per inch. Distribution of the clock pulses within the unit itself presents problems, though not of the magnitude presented in the transmission line which must supply power to all cores simultaneously.

The method for the distribution of power pulses within the unit is again an extension of the parallel flat-conductor principle, but here the parallel conductors have been expanded into a laminated structure of five conducting sheets with insulation between each foil sheet. Each sheet carries a different power pulse, and

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turret lugs spaced symmetrically on the structure make contact to the separate sheets. Each core socket is surrounded by terminals to any one of the four power pulses required, keeping lead length of the clock lines to a minimum.

This type of construction offers another advantage. So far all effort has been geared toward keeping the power distribution lines to low inductances, but it is just as important to have low inductance in the output lines of the magnetic amplifiers since these lines also carry relatively large currents.

The laminated structure described inherently provides a ground plane for all currents. If the wiring between cores is spaced closely to the clock distribution sheets, then the circuit loops are small and the inductance is low. It should be pointed out that for a unit of this size and power level the pains taken with the distribution system are not necessary. However, the method employed is in the right direction for handling low-impedance circuits, and appears adaptable to mass-production techniques such as stamped or printed construction.

A block diagram of the accumulator is shown in Fig. 5. It consists of a unit adder and a four-bit circulating register. Provision is made to add in unity each time a push button is pressed, and for the accumulated count to be displayed by means of incandescent lamps powered directly from cores. Thirty-seven cores are used altogether, 12 being used in the adder and register, the other 25 used for cycling and input and output synchronization.

The cycling unit presents every twelfth pulse to the gate G which is enabled when the ADD button is depressed. The synchronizing unit ignores the first input pulse since it may be marginal, and presents the second input pulse to the adder while closing the gate by means of the lockout flip-flop to prevent further input signals. Releasing the ADD button opens gate G and resets the lockout flip-flop.

Since the register is circulating, the contents may be sampled only once every four pulse-times to display the contents. The indicator lamps are therefore only energized on an approximate 10 per cent duty cycle, but still provide enough illumination for display purposes. Fig. 6 shows the complete unit.

At this frequency each core is capable of driving three to four other cores. Non-critical components have been used in the unit, with each core having an allowable flux variation of ±5 per cent, and all resistors being ±10 per cent stock-value carbon resistors. Satisfactory operation is obtained over a clock voltage range of 18 to 25 volts. The clock source is a single oscillator tube.

The clock input power is approximately 15 watts, or 400 milliwatts per core. An additional 10 watts of d-c power is used to supply clamp voltages. As each core is a complete logical element, the total input power is only 606 milliwatts for each gate or buffer, which compares very favorably with any other type of computer circuitry. As was pointed out earlier, this unit was constructed only to test the operation of magnetic amplifiers in the megacycle range. The unit has shown that operation at 2.5 megacycles using practical tolerances and components is feasible.

Discussion

R. E. Montijo (Radio Corporation of America): What advantages do you claim for the magnetic circuits described over functionally comparable transistor circuits?

Mr. Torrey: Comparable transistor circuits capable of driving three or four others at an information rate of 2.5 megacycles are not very common at present and are fairly expensive. However, this situation will certainly improve. The attractive features of magnetic amplifiers are their long life expectancy and relative lack of sensitivity to environmental conditions, particularly temperature, humidity, and electrical noise. Also, where high speed is combined with high power levels, such as driving coincident-current memories or heavily loaded busses, magnetic amplifiers can perform functions impossible with presently available transistors.

K. Preston, Jr. (Bell Telephone Laboratories): What type of diodes are used in your circuitry?

Mr. Torrey: The diodes used are germanium diodes with low-forward voltage drop. The output diodes are further characterized by being the so called "fast recovery" type and are of gold-bonded construction. Several manufacturers make these types of diodes for computer applications.

E. Cohler (Sylvania Electric Products): What is the "add" time of the 2.5-megacycle accumulator?

Mr. Torrey: Being a serial adder, the addition time is dependent upon word length. The adder has three cascaded stages, and produces a 0.6 microsecond delay from input to output. However, being serial, digits can be fed to the adder at a 2.5 megacycle rate.

J. C. Lozier (Bell Telephone Laboratories): Since your amplifier does not regenerate each pulse, what limitations does this place on logical design, reliability of pile up, and so forth?

Mr. Torrey: The pulses are reshaped and relocked in each stage by means of the regularly recurring power pulse. Regeneration is not used, but if a signal is above a certain critical amplitude, in a long chain of amplifiers, it will grow to be a full amplitude pulse. The limitations put upon the logical designer are:

1. As this is a 2-phase synchronous system, he must keep track of phase and of delays to insure that the signal arrives at its destination in the right phase and at the right time.
2. The logical designer must not load the output of any stage so heavily that there is a chance the output may fall below the critical level, and thus be attenuated as it progresses from stage to stage.