Adaptive Signal Processing Algorithms using Sigma Delta Architectures

J. Juni, R.W. Stewart
Signal Processing Division
Department of Electronic and Electrical Engineering
University of Strathclyde
Glasgow G1 1XW, UK
E-mail bob@spd.eee.strathclyde.ac.uk

Abstract

Using oversampled sigma-delta ($\Sigma-\Delta$) techniques a signal can be represented as a single bit binary data stream ({-1, 1}), with the quantization noise high pass filtered out of baseband. In this paper adaptive LMS digital filters are presented that directly use binary $\Sigma-\Delta$ input streams and update the PCM adaptive filter weights at the oversampled rate to realize architectures that are very suitable for mixed analog/digital VLSI implementation. Using the $\Sigma-\Delta$ adaptive architecture PCM values are multiplied by single bits, and can therefore be easily performed by a simple multiplexor. Also using the $\Sigma-\Delta$ approach, the decimation and interpolation stages required for converting from $\Sigma-\Delta$ to PCM (and vice-versa) suitable for Nyquist DSP algorithms are circumvented. The paper will describe the sigma delta adaptive LMS filter architecture and present preliminary results for adaptive echo cancellation using adaptive sigma delta and standard PCM architectures.

1. Introduction

In the last few years oversampled DSP systems have emerged as cost effective and high quality solutions for a number of application areas such as digital audio. Recently oversampling sigma delta ($\Sigma-\Delta$) ADCs and DACs have become available that allow cost effective single chip (mixed analog/digital) DSP solutions, by virtue of the minimal analog requirements of $\Sigma-\Delta$.

1.1 Oversampling Analogue Filter Specification

Oversampling a signal with Nyquist rate of f_s, at an oversampled frequency of f_{ovs}, also allows *cheaper* DSP systems to be realized because the specification of the anti-alias and reconstruction filters can be reduced by implementing digital low pass filters cutting off at half the Nyquist rate ($f_s/2$). Therefore an analog filter that has a flat frequency response up to $f_s/2$, and a slow roll-off to the stopband at $f_{ovs}/2$ is required. The Nyquist rate analog filter would require a very sharp cut-off at $f_s/2$ and is therefore expensive.

1.2 Oversampling to Increase Signal Resolution

As well as reducing the cost, oversampling can be used to increase the resolution of an ADC or DAC (assuming that the noise floor of the device is low enough). If an ADC has a quantization level of q volts the in band quantization noise power, Q_N, is well known to be:

$$Q_N = \frac{q^2}{12} \tag{1}$$

From Figure 1 it can be seen that oversampling a signal by a factor of 4 times the Nyquist rate reduces the in-band quantization noise (assumed to be a flat spectrum between 0 Hz and $f_s/2$ Hz) by 1/4. This noise power is equivalent to an ADC with step size $q/2$ and hence baseband signal resolution has been increased by 1 bit [8]. In theory if a single bit ADC with an appropriately low noise floor were used and oversampled by a factor of 4^{15} ($\approx 10^9 \times f_s$) then a 16 bit resolution signal could be realized. Clearly this sampling rate is not practically realizable.

1.3 Quantization Noise Shaping Techniques

By using $\Sigma-\Delta$ noise shaping techniques the in-band quantization noise from oversampling can be high pass filtered, and the oversampling factor required to increase signal resolution can be reduced. Figure 2 shows a simple first order $\Sigma-\Delta$ modulator. Using a 64 × 's oversampling 3rd order sigma delta converter to produce a single bit stream signal will yield *more than* 13 bits of resolution in the baseband signal [1], [2], [7].

2. Sigma Delta DSP Architectures

$\Sigma-\Delta$ ADCs [1], [7] produce a binary ({-1,1}) data stream at oversampled rates such that the quantization

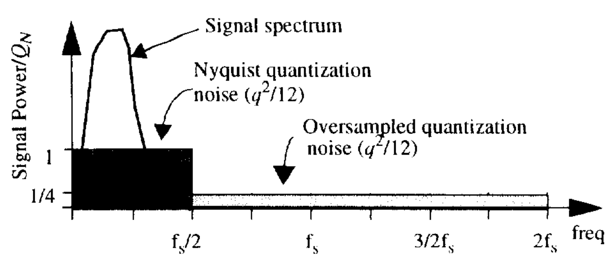

Figure 1: Oversampling a signal to increase resolution.

noise is high pass filtered, but the baseband signal of interest is relatively unaffected. As an example, Figure 3 illustrates the time and frequency domain representations of a sum of two sine waves sampled at Nyquist rate and at a 16 × 's oversampled rate using a Σ–Δ converter.

Σ–Δ ADCs and DACs are very suitable for VLSI implementation as they do not require precision analog components, unlike conventional high precision ADCs which may require very accurately laser trimmed components. The analogue circuitry required for the simple (first order) Σ–Δ ADC in Figure 2 is a comparator, a single bit DAC and capacitive (integrating) components, all of which can be cost effectively implemented in mixed analog/digital CMOS devices [1].

When using Σ–Δ ADCs and DACs for analog input/output to a general purpose DSP microprocessor system computing with Nyquist PCM data and algorithms, decimation and interpolation stages are required to convert the data to and from standard PCM (pulse coded modulation) at the Nyquist rate as shown in Figure 4 [9].

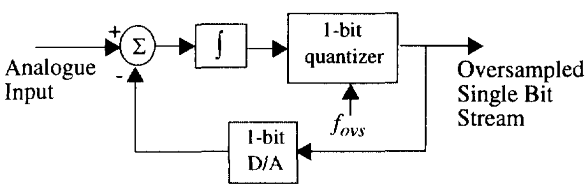

Figure 2: First order Σ–Δ converter.

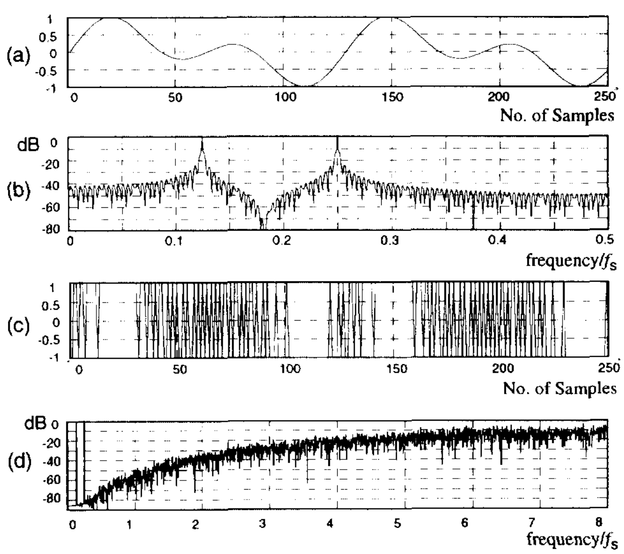

Figure 3: 0.1Hz + 0.2Hz sine wave sampled at f_s=1Hz (a) PCM time domain (b) PCM frequency domain; (c) 16 x's oversampled 1 bit Σ–Δ time domain; (d) 16 x's oversampled frequency domain.

2.1 Sigma Delta Based FIR Filters

Recently it has been suggested that because a Σ–Δ bit stream is the signal plus the shaped quantization noise (see Figure 3), then this data stream at the oversampled frequency can be used as the input to a PCM coefficient FIR filter as shown in Figure 5 [2]. Similarly the weights of the FIR filter can be oversampled and Σ–Δ coded, and oversampled PCM data is input, or both data and filter weights can also be encoded as single bit Σ–Δ signals. (IIR sigma delta implementations have also been reported [4]).

To appreciate that the filter of Figure 5 will perform correctly recall that convolution in the time domain is multiplication in the frequency domain and hence the out of baseband noise in the oversampled input signals will not affect the baseband filter output. (More formal arguments can be found in [2].) The oversampled FIR filter output can then be decimated to PCM at the Nyquist rate, or directly output by a suitable Σ–Δ DAC after the signal is requantized to single bit using an all digital Σ–Δ stage.

Implementing an FIR filter using a Σ–Δ architecture has the advantages that the decimation (Σ–Δ to PCM) and interpolation (PCM to Σ–Δ) stages are circumvented, and a mixed analog/digital VLSI solution is possible due to the straightforward digital circuitry of adders and one bit by M-bit multipliers (performed by a multiplexor function) and the implementation of the Σ–Δ devices in CMOS. Therefore, given the advantages for FIR filters, it would

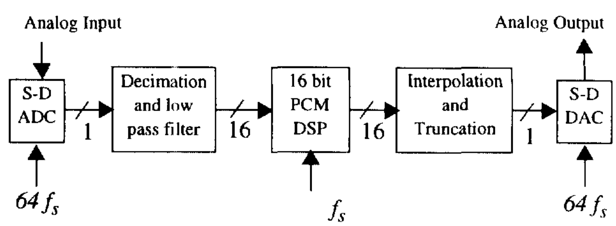

Figure 4: Using Σ-Δ devices for Nyquist rate DSP algorithms.

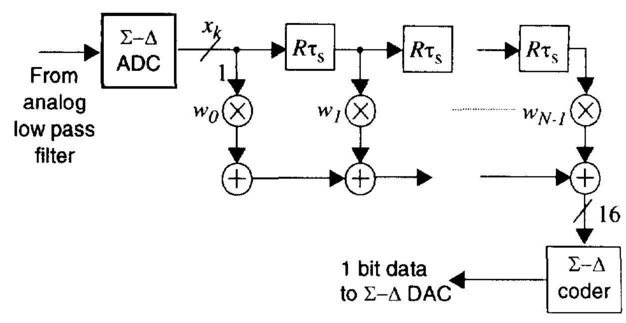

Figure 5: FIR Filters operating with Sigma delta data and PCM coefficients.

also seem attractive to implement *adaptive* FIR filters using Σ–Δ architectures.

3. Adaptive DSP using Sigma Delta

The general gradient equation for finding the minimum mean squared error solution for the general adaptive signal processor in Figure 6 is given by:

$$w_{k+1} = w_k + \mu(-\nabla_k) \quad (2)$$

where the filter output is calculated by:

$$y_k = w_k^T x_k \quad (3)$$

and the error is simply:

$$e_k = d_k - y_k \quad (4)$$

w_k is the FIR filter N weight vector, x_k is the input data vector of the last N filter inputs, μ is the step size, d_k the desired signal, and ∇_k is the gradient vector such that:

$$\nabla_k = \frac{\partial}{\partial w_k} E(e_k^2) \quad (5)$$

The well known LMS algorithm estimates the gradient ∇_k, as the gradient of the instantaneous error, such that:

$$\hat{\nabla}_k = -2 e_k x_k \quad (6)$$

and the simple LMS FIR filter weight update [6] is realized:

$$w_{k+1} = w_k + 2\mu e_k x_k \quad (7)$$

If the input signal, x_k, and the desired signal, d_k, were oversampled binary Σ–Δ encoded and the filter weights were oversampled M-bit PCM coefficients, then the output

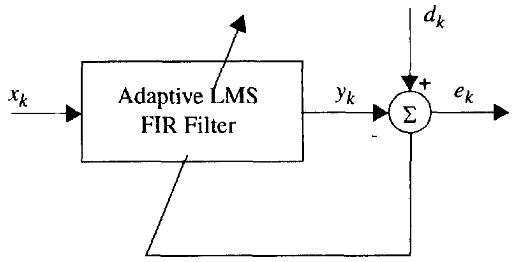

Figure 7: General model for adaptive signal processing using the LMS algorithm

of the filter, y_k, would be an oversampled signal of up to M bits. It would appear then that the LMS update Eq. 7 could be implemented with only single bit multiplies, given that e_k is an M bit oversampled signal, and x_k is binary. One disadvantage of this approach is that the number of M-bit coefficients is very high; a factor of the oversampling ratio higher when compared with the number in the Nyquist FIR. (It is worth noting that a form of this Σ–Δ adaptive LMS filter is reported in [10] where Eq. 4 is implemented by an analog circuit, and then input to a Σ–Δ converter for input to the adaptive filter).

If the adaptive filter PCM coefficients were *not* oversampled (i.e. zeros inserted) then the hardware requirements could be reduced. However the convergence of the LMS is inhibited by the uncorrelated high frequency out of baseband Σ–Δ quantization noise present on both x_k

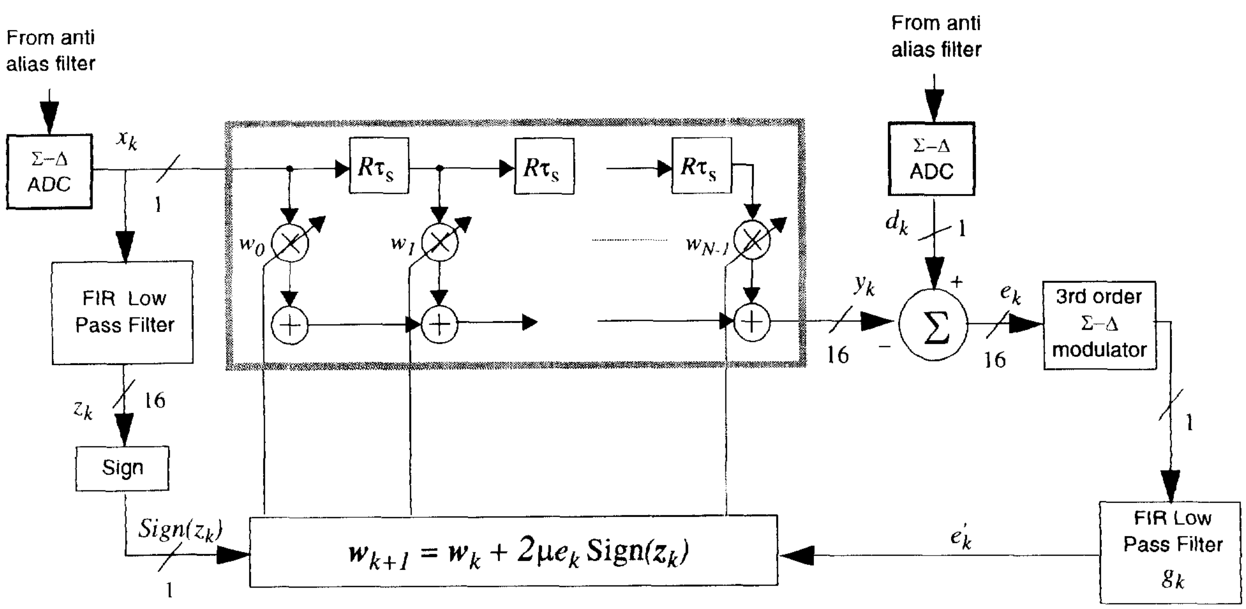

Figure 6: Sigma delta architecture for adaptive LMS algorithms.

and d_k. However by filtering out the high frequency noise a solution is possible, as shown in Figure 7. Both input and desired data are single bit $\Sigma-\Delta$ encoded at an oversampling frequency of f_{ovs}. The oversampling ratio is R, i.e. $f_{ovs}= Rf_s$. The adaptive FIR filter weights are baseband PCM (i.e. *not* oversampled). The x_k and d_k $\Sigma-\Delta$ binary data streams have two levels of quantization equivalent to 2^{-M} and 2^{M} on the PCM signal scale. When $e_k = d_k - y_k$ is formed the output is a multi-bit PCM oversampled signal, given that y_k is a multibit oversampled signal. Therefore an all digital 3rd order $\Sigma-\Delta$ section is used to convert the oversampled 16 bit signal to an oversampled single bit data stream. The out of band quantization noise is then removed from e_k' using a low pass FIR filter (20 weights) stage requiring only single bit multiplies [8]. Note therefore that the error signal made available to the LMS has now been convolved with the comb filter impulse response g_k. Therefore:

$$e_k' = (d_k - y_k) * g_k \tag{8}$$

and the LMS update will require to be *re*-derived.

3.1 Filtered-X Architecture

Recalling that the LMS uses the instantaneous gradient of the squared error, then we can show that:

$$\hat{\nabla}_k = -2e_k'z_k \tag{9}$$

where,

$$z_k = x_k * g_k \tag{10}$$

and z_k is a vector of the last N z_k values. The data vector must therefore also be filtered by the same filter as used for the error signal, which also removes the out of baseband noise from x_k. (This algorithm is in fact similar to the filtered-X LMS [6].) The $\Sigma-\Delta$ LMS update is therefore:

$$w_{k+1} = w_k + 2\mu e_k z_k \tag{11}$$

However, because e_k and z_k are both multibit signals this architecture would require the provision of a multibit multiplier. As it is desirable that there is only single bit multiplication, then Eq. 11 is simplified to the sign data LMS where only the sign of z_k is retained. Hence the LMS update used in Figure 7 is now:

$$w_{k+1} = w_k + 2\mu e_k \text{Sign}(z_k) \tag{12}$$

By taking the sign of the each element in the data vector z_k the multiplication of e_k and x_k can be performed as N single bit operations. (A signed error approach could also be used, however sign data reduces the algorithm storage requirements and was therefore chosen.) Eq. 12 is updated at the oversampled data rate of f_{ovs}, again noting that the weight vector, w_k, is PCM encoded (and not oversampled). It is well documented that the sign data algorithm will not converge as rapidly, or to as small a mean squared error as the normal LMS. However we have noted that by extending the precision of the weight vector to 20 bits, we can produce results that greatly improves convergence and MMSE for the sign data algorithm. This technique will be the subject of a more detailed future publication.

4. Sigma Delta LMS for Echo Cancellation

An echo cancellation example will be used to demonstrate performance of the sigma delta LMS. The performance of the sigma delta approach will be compared to conventional 16 bit PCM adaptive signal processing. The input signal, x_k, was white noise with the standard deviation set to 1/4 of the full scale for the standard PCM, and to 1/12 of the full scale for $\Sigma-\Delta$. The oversampling ratio was $R = 32$, and the echo model had the impulse response shown in Figure 8. The adaptive filter length was 80 weights in both cases.

Figure 9 shows the ensemble mean squared error for 20 simulations of (a) standard PCM adaptive LMS, (b) the 16 bit PCM adaptive weight $\Sigma-\Delta$ and (c) the 20 bit PCM adaptive weight $\Sigma-\Delta$. Although the results are only illustrative, rather than conclusive, it is clear that the $\Sigma-\Delta$ LMS can match the performance of the standard PCM approach when 20 bit adaptive weights are used.

5. Conclusions and Current Work

This paper has developed and demonstrated the performance of an all digital $\Sigma-\Delta$ adaptive FIR LMS filter. The implementation is suitable for mixed analog/digital implementation, and work is currently underway to formally show that a semi-custom $\Sigma-\Delta$ adaptive LMS will use considerably less hardware than a semi-custom PCM implementation. Simulations suggest that with the appropriate choice of step size the architecture is stable, and can *almost* match the performance of standard adaptive DSP with PCM coefficients and data. We are also developing a demonstration of the technique for V.32 standard echo cancellation and equalization using the complex LMS.

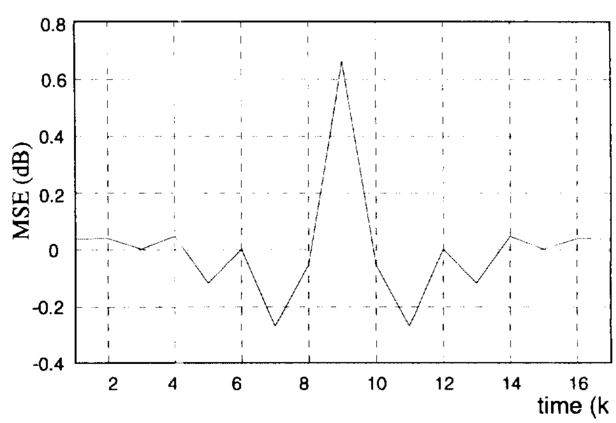

Figure 8: Impulse response of simulated echo channel.

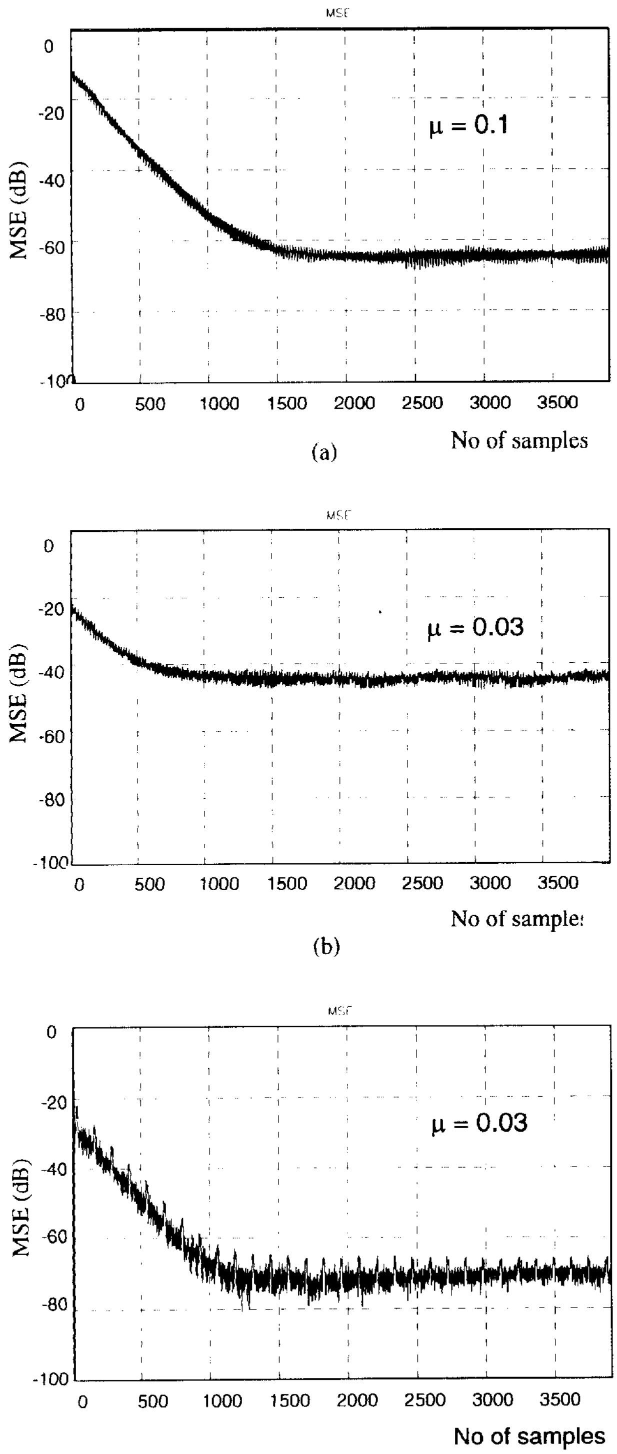

Figure 9: Ensemble mean square error (MSE) (20 simulations) for echo cancellation using (a) standard 16 bit PCM, LMS; (b) Σ–Δ LMS with 16 bit weights; (c) Σ–Δ LMS with 20 bit weights.

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