A Mixed-Signal Decision-Feedback Equalizer Using a Look-Ahead Architecture

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ABSTRACT

A mixed-signal decision-feedback equalizer (DFE) that uses a look-ahead architecture is described. This look-ahead DFE doubles the data rate using parallelism with less than a doubling of the circuitry. Since much of the signal processing is carried out in the analog domain, nonidealities associated with the analog signal processing are considered.

INTRODUCTION

Decision-feedback equalization is a viable method of removing inter-symbol interference (ISI) produced by a disk-drive read channel [1,2,3] or other communication channels [4]. The decision-feedback equalizer (DFE) in combination with a linear forward equalizer has advantages over a linear equalizer alone, such as less sensitivity to timing phase and smaller mean-squared error (MSE) [5]. Figure 1 shows the block diagram of a complete hard-disk read channel that uses a DFE. The read electronics contains many components in addition to the DFE: timing recovery, forward equalizer, automatic gain control (AGC), and preamp.

This paper focuses on a mixed-signal implementation of the DFE for a disk-drive read channel. A mixed analog-digital implementation has some advantages when compared to a digital implementation. Digital implementations of read channel equalizers require a medium-resolution analog-to-digital converter (ADC) early in the signal path [6]. The ADC is often placed after the AGC and a bandlimiting filter; therefore the forward equalizer, timing recovery and DFE are implemented digitally. The ADC is typically a 6-bit flash ADC that is composed of 63 comparators. In contrast, a completely analog read channel equalizer does not require a front-end flash ADC. The mixed-signal DFE does require a small ADC to generate decision and error signals, but this ADC may only need 3 to 5 comparators. Also, a digital finite-impulse-response forward equalizer requires digital convolution multipliers that consume large area and power. In contrast, an analog forward filter can be smaller and lower power.

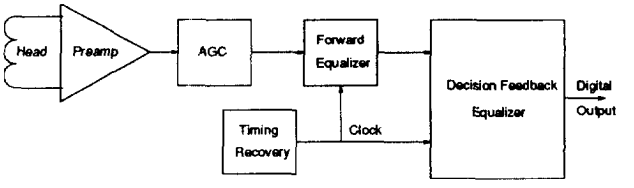

Figure 1: Disk-drive read channel block diagram

Our goal is to design a high-speed, mixed-signal DFE in a CMOS technology for future disk-drives and other communication applications. In this paper, a mixed-signal look-ahead DFE is described that uses parallelism to achieve an increase of the data rate. In the next two sections, a mixed-signal DFE is described. Then the look-ahead DFE is presented.

DECISION FEEDBACK EQUALIZATION

The forward equalizer in Figure 1 is responsible for removal of pre-cursor ISI. The DFE removes the remaining post-cursor ISI by using a linear combination of past decisions to cancel the interference [1]. Figure 2 shows an adaptive DFE architecture. Since the signal is sampled by the slicer at bit times nT, the post-cursor ISI, ISI^+, need only be canceled at those discrete times. The ISI^+ at time nT can be expressed as a weighted summation of past bits:

$$ISI^+(n) = h_{offset} + \sum_{k=1}^{M} h(k)\hat{y}(n-k) \,, \qquad (1)$$

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where $\{h(k)\}$ is the impulse response of the disk channel plus forward equalizer sampled at times kT, $\{\hat{y}(n-k)\}$ is the past decisions, and h_{offset} is the d.c. offset. M is the number of bits that contribute significant post-cursor ISI.

The sequence $\{h(k)\}$ must be determined and used as the coefficients $\{d_k\}$ of the DFE in order to cancel the ISI^+. The coefficients are determined by adapting the DFE using an algorithm which minimizes the mean-square value of the error $e(n)$, where $e(n) = \hat{y}(n) - \tilde{y}(n)$ is the error across the slicer. Once the DFE has adapted, the coefficients are

$$d_k = -h(k) \text{ for } 1 \le k \le M \qquad (2)$$

and

$$d_0 = -h_{offset}, \qquad (3)$$

where d_k is the coefficient at tap k, d_0 is the d.c. offset cancellation coefficient, and M is the number of taps. With these conditions satisfied, the ISI^+ is canceled by the DFE.

Figure 2 shows a five-tap DFE. Four taps cancel post-cursor ISI, and one tap cancels the d.c. offset. Based on simulations using a Lorentzian channel model [1] with $PW_{50} = 2T$ and appropriate forward equalization, a five-tap DFE is sufficient to meet our specification of MSE < -25 dB with a noise-free channel, where MSE = $E(e^2(n))$ [7].

The DFE coefficients can be adapted after each decision using the LMS algorithm [8]:

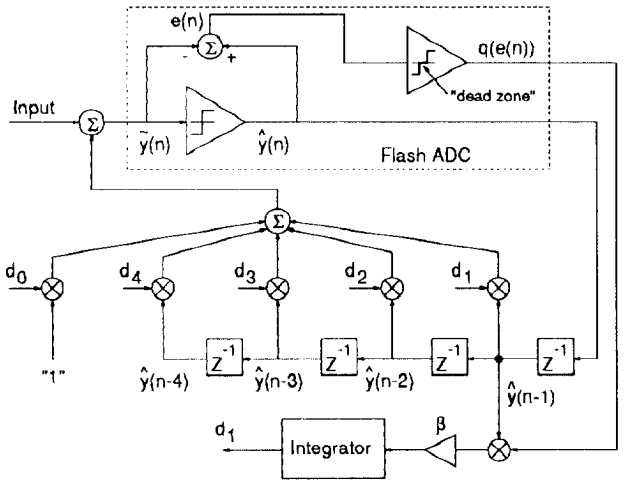

Figure 2: Adaptive DFE with modified LMS update shown for coefficient d_1. Z^{-1} is a delay of one bit period T.

$$d_k(n+1) = d_k(n) + \beta e(n)\hat{y}(n-k) \text{ for } 1 \le k \le M \qquad (4a)$$

$$d_0(n+1) = d_0(n) + \beta e(n), \qquad (4b)$$

where $\beta << 1$ is the gain of the update integrator.

In steady state, $d_k(n) \approx constant$ and the time average of $e(n)\,\hat{y}(n-k)$ in (4a) is approximately zero, indicating that there is no correlation between the error and the delayed decision and that the coefficients are optimal. Similarly, when $d_0(n) \approx constant$, the time average of $e(n)$ in (4b) is approximately zero indicating that there is no offset at the input to the slicer (assuming that the data is zero mean).

A modification and simplification of the LMS algorithm uses the sign of the error in (4) for updating the coefficients [4]. By using the sign of the error signal, the integration in (4) can be implemented by a L-bit up-down counter if $\beta = 2^{-L}$ because $\text{sign}(e(n))\,\hat{y}(n-k)$ is either +1 or −1. As a further modification, a three-level error signal, $q(e(n))$, can be used that equals zero when the magnitude of the error is sufficiently small (and falls in a small "dead zone") and equals $\text{sign}(e(n))$ otherwise. This $q(e(n))$ takes on values $\{-1,0,1\}$. Equation (4) shows that zero error produces no change in the coefficients. The decision $\hat{y}(n)$ and $q(e(n))$ can be generated by a simple flash ADC as shown in Figure 2. The modified LMS update for coefficient d_1 is also shown in Figure 2.

MIXED-SIGNAL DFE ARCHITECTURE

Figure 3 shows our first mixed-signal DFE [7]. The look-ahead DFE architecture that is described in the next two sections is based on this architecture. The input is an analog current coming from a preceding analog forward equalizer [9,10,11,17]. A current-to-voltage (I2V) converter feeds the small flash ADC which outputs the binary decision $\hat{y}(n)$ and quantized error $q(e(n))$ using only 5 comparators.

Counters are used as the integrators in the modified LMS algorithm. The quantized error $q(e(n))$ and the past decisions $\hat{y}(n-k)$ are mapped to control signals for the counters. The digital output of the counters feed voltage-mode digital-to-analog converters (DACs) that drive current-output multipliers [12]. Each DAC uses a resistor ladder and CMOS switches to output a voltage that is the coefficient value. The multipliers perform the multiplication of the digital signal $\hat{y}(n-k)$ by the analog coefficient value d_k. The current outputs are all summed at the I2V input simply by connecting them together.

One key difference between an analog implementation of a DFE and a digital implementation is

the nonidealities associated with analog circuits. Analog components in the forward equalizer and DFE generate a d.c. offset which will shift the d.c. level at the input to the ADC and degrade the performance of the DFE. A coefficient d_0 is included to cancel the d.c. offset, as shown in Figures 2 and 3. Some nonlinear effects in the analog convolution multipliers are also canceled by d_0 [13].

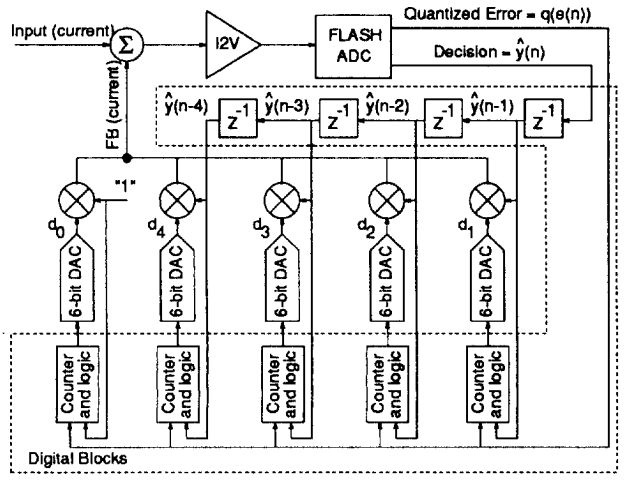

Figure 3: Mixed-signal DFE showing analog and digital circuit blocks. The digital blocks are enclosed by the dashed line.

Behavioral simulations of the DFE have shown that the coefficients in (4) require ten-bit resolution. However, the convolution calculation in (1) requires only six-bit coefficient resolution to assure that the ISI^+ cancellation meets the –25 dB MSE specification. Therefore, the coefficients are stored as ten-bit binary numbers in the counters and then quantized to six bits before being latched by the 6-bit DACs.

Behavioral simulations also indicate that the flash ADC needs at least six bits of linearity to assure MSE<– 25 dB. Through simulations, it was determined that the small nonlinearity introduced by the analog convolution multipliers does not have a measurable effect on the MSE achieved by the DFE.

LOOK-AHEAD DFE CONCEPT

The critical, speed-limiting feedback loop in Figure 3 is through the I2V converter, flash ADC and d_1 multiplier. This feedback loop must have a total delay less than one bit period, T. Although shown as a separate delay element, most of the Z^{-1} delay in this critical loop is in the flash ADC. To reduce T and thereby increase the data rate of the DFE, either the speed of these circuits must increase or parallelism can be used.

Parallelism is used in the look-ahead (LA) DFE to change the critical, speed-limiting feedback loop to being through the d_2 multiplier rather than the d_1 multiplier [14]. The key assumption here is that the delay through the flash ADC is longer than the critical feedback loop delay of one bit period T (Z^{-1}). (Typically, the comparators in the flash ADC are slower than the other circuitry.) Since the delay through the ADC exceeds T, the previous decision $\hat{y}(n-1)$ is not available for the convolution calculation to compute ISI^+ at time n. Therefore, two convolution values are computed in the LA DFE, one for each possible value of $\hat{y}(n-1)$. These computations are done in parallel paths in the LA DFE.

The LA DFE can be explained conceptually using the simplified diagram in Figure 4. For clarity, the error signal is not shown and the flash ADC is shown simply as a slicer. There are two parallel processing paths in the LA DFE. Each path is a copy of the DFE of Figure 2 with the following changes. The upper path always assumes $\hat{y}(n-1)=+1$ and uses that value in its convolution calculation. The lower path always assumes and uses $\hat{y}(n-1)=-1$. Both paths use the same d_k coefficients and the same (correct) values of $\hat{y}(n-2)$, $\hat{y}(n-3)$ and $\hat{y}(n-4)$ in the convolution calculation. The two parallel paths produce inputs to the upper and lower slicers that output two tentative decisions $\hat{y}_{+1}(n)$ and $\hat{y}_{-1}(n)$, where $\hat{y}_{+1}(n)=[\hat{y}(n)$, if $\hat{y}(n-1)=+1]$ and $\hat{y}_{-1}(n)=[\hat{y}(n)$, if $\hat{y}(n-1)=-1]$.

Selection between tentative decisions $\hat{y}_{+1}(n)$ and $\hat{y}_{-1}(n)$ can made using $\hat{y}(n-1)$. However, as shown in

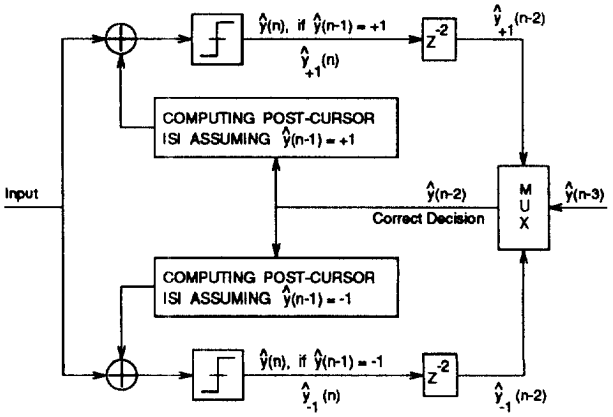

Figure 4: Conceptual block diagram of the LA DFE. The tentative decisions experience delay in the ADCs that output the decisions.

Figure 4, this selection must wait for a delay of $2T$. During this delay time, the tentative decisions are essentially 'stuck' inside the ADC and are not available. Taking into account this extra delay, the selection is actually made between the delayed tentative decisions $\hat{y}_{+1}(n-2)$ and $\hat{y}_{-1}(n-2)$, with the selection determined by the value of $\hat{y}(n-3)$. At start-up, a training sequence of known data is used for rapid and reliable convergence [4]. This sequence of known data initializes the selection process, giving known values for the select signal $\hat{y}(n-3)$ during the training data. At the end of the training data, the selection process can operate using the correct delayed decision that is output by the LA DFE.

In the LA DFE, the critical, speed-limiting feedback loop now must have a total delay less than $2T$. The loop delay of $2T$ is represented by the Z^{-2} block in Figure 4. More than half of the loop delay ($>T$) is in the flash ADC and the rest ($<T$) is in the mux, d_2 multiplier, and I2V.

LOOK-AHEAD DFE

A block diagram of the LA DFE is shown in Figure 5. The LA DFE uses the same circuit blocks that are used in Figure 3. The critical feedback loop is through the d_2 multiplier, which allows a total delay of $2T$ through the I2V, flash ADC and multiplier. A flash ADC with pipelined comparators [15] is used in each of the upper and lower paths to allow decisions to be made at a $1/T$ rate, with a delay less than $2T$ through each ADC. The decision delay line and LMS update circuitry (not shown) are shared by the two paths. The update circuitry can be shared because only the selected, correct past decisions and error signal are used to update the coefficients. This sharing saves both power and IC area.

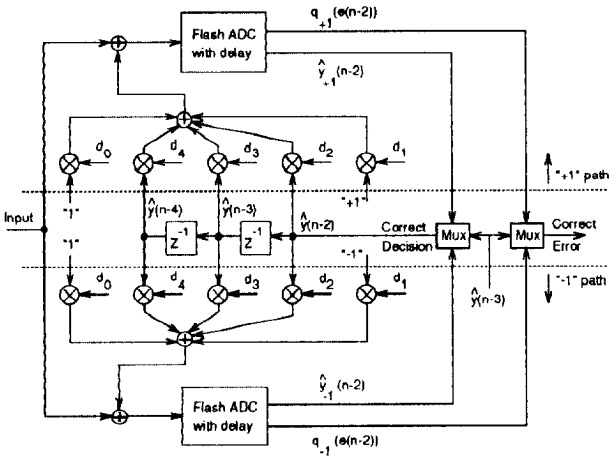

Figure 5: LA DFE block diagram. LMS update hardware is not shown.

Due to the delay in the ADC, the signals $\hat{y}(n-1)$ and $q(e(n))$ are not available to update the coefficients at time n. Therefore, a delayed version of the LMS coefficient update algorithm [16] is used:

$$d_k(n+1) = d_k(n) + \beta q(e(n-2))\hat{y}(n-k-2) \quad \text{for } 1 \le k \le M \qquad (5a)$$

$$d_0(n+1) = d_0(n) + \beta q(e(n-2)) \qquad (5b)$$

Two additional delay elements (not shown in Figure 5) are required to hold past decisions $\hat{y}(n-5)$ and $\hat{y}(n-6)$ which are used for updating coefficients d_3 and d_4 respectively.

The two parallel paths in the LA DFE must be identical in order to achieve the same performance as the conventional DFE. In reality, the analog circuits in these paths will be mismatched to some extent. Two mismatches are d.c. offset mismatch and convolution-path gain mismatch. In Figure 6, $1+g\_p$ and $1+g\_n$ model the gain of each convolution path, and *offsetp* and *offsetn* model the d.c. offset of each path.

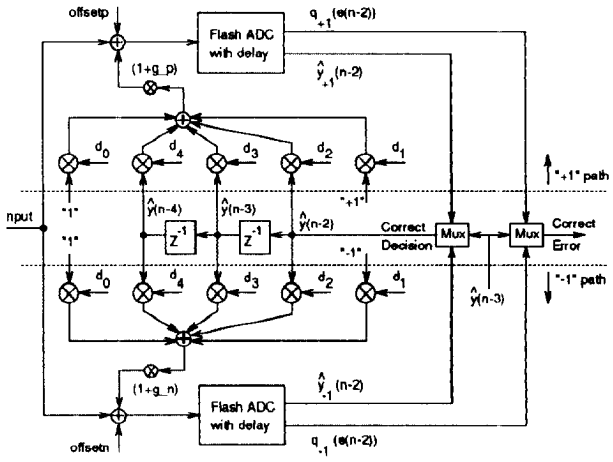

Figure 6: LA DFE block diagram modeling d.c. offsets and convolution-path gains.

The coefficient d_0 in Figure 6 adapts to cancel the average d.c. offset, (*offsetp* + *offsetn*)/2, and d.c. offset mismatch, (*offsetp* – *offsetn*), is canceled by the d_1 coefficient along with the ISI caused by $\hat{y}(n-1)$. The fact that d_1 cancels offset mismatch can be explained as follows. For simplicity, assume there is no ISI and that the average d.c. offset is zero (so that all $d_i = 0$ except d_1), $g\_p = g\_n = 0$, and *offsetp* = –*offsetn* = Δ. Under these conditions, the tentative error values produced by the two paths are $e_{+1}(n-2) = -\Delta - d_1$ and $e_{-1}(n-2) = \Delta + d_1$. The

selected error $e(n-2)$ is either $e_{+1}(n-2) = -\Delta - d_1$ when $\hat{y}(n-3) = +1$ or $e_{-1}(n-2) = \Delta + d_1$ when $\hat{y}(n-3) = -1$. Using these values, the update equation for d_1 (using (5a) without quantizing the error) becomes

$$d_1(n+1) = d_1(n) + \beta e(n-2)\,\hat{y}(n-3)$$
$$= d_1(n) - \beta(\Delta + d_1(n)), \qquad (6)$$

When $d_1 = -\Delta$, d_1 reaches steady state. When ISI is present, d_1 adapts to cancel Δ and the ISI due $\hat{y}(n-1)$. A similar analysis shows that d_0 cancels the average d.c. offset of the two paths.

A custom-written C program was developed to evaluate the effect of offset and gain mismatches on the performance of the LA DFE. Based on these simulations and the requirement that MSE<–25 dB, the LA DFE can compensate for average d.c. offsets of ±0.5V and d.c. offset mismatch of ±0.4V, where the binary data amplitudes are ±1V. The LA DFE can tolerate ±0.10 convolution-path gain mismatch ($g\_p - g\_n$). The average convolution-path gain deviation, $(g\_p + g\_n)/2$, is compensated during adaptation by scaling all coefficients by a common factor.

CONCLUSION

A mixed-signal look-ahead DFE was presented that increases the data rate by a factor of two by using parallelism. Area increase due to the parallelism is less than a factor of two because the duplicated blocks are small and not all circuits must be duplicated. Based on simulation results, the LA DFE is insensitive to d.c. offset and gain mismatches that might arise in the analog circuitry.

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