A Single Processor Packet Radio Modem for Land Mobile Vehicle Tracking Applications

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Abstract

Data communication over VHF/UHF land mobile radio channels presents a difficult, yet well understood, set of technical challenges. These challenges include time-varying multipath profiles, Rayleigh fading, and low to moderate signal-to-noise ratio. Modem designs must support additional application based constraints including rapid synchronization, spectrally efficient modulation, a reliable over-the-air protocol, and relatively low cost. The cost constraint, along with an interest for easy support and upgradability, motivated a single DSP processor radio modem design that supports both control and modem applications. An implementation of such a modem is described which meets all of the design criteria.

I. Introduction

Since Murota and Hirade [1] first summarized its potential benefits for the land mobile radio channel, a number of authors [2],[3],[4],[5] have described both the theoretical performance and operational architecture of modem designs using GMSK modulation. However, in many applications, it is either the cost constraint or practical considerations that ultimately drive the final system design. The overwhelming majority of VHF/UHF mobile radio systems in use today were designed with analog voice in mind. Transitioning these systems to include data communications implies the practical constraint of using the existing narrowband FM radio transceiver already in place in a vehicle. These radios typically use direct FM modulation and noncoherent FM discriminators operating in 5 kHz to 25 kHz channel bandwidths. Using this radio scenario, the design goal was work within these design constraints while minimizing overall end-to-end cost.

The system described here is a single processor baseband modem design for GPS-based vehicle tracking applications. It is optimized to provide the highest data throughput with an acceptable bit error rate. DGMSK modulation was chosen due to its high spectral efficiency. Superior bit error performance was achieved by adding Reed-Solomon block forward error correction.

Section II describes the overall system design considerations. Section III describes the hardware platform. The software architecture and key algorithm designs are reviewed in Section IV. The modem performance is presented in Section V. Section VI provides concluding remarks.

II. Design Considerations

The major applications-based constraints for the design are as follows:

- Half-duplex in-vehicle modem
- Full-duplex base station modem
- Compatibility with VHF/UHF FM mobile radios operating in 5 kHz, 12.5 kHz, or 25 kHz channels
- Direct FM modulation and noncoherent discriminator detection
- Average vehicle speeds from 10 km/h to 40km/h

External design requirements resulted in a specification of -95dBm minimum signal level at either the base station or mobile receiver. The multipath delay spreads for urban and high rise channels are generally less than 10 microseconds and typically between 0-5 microseconds. This implies that the coherence bandwidth is at least 100 kHz. With the widest required signal bandwidth less than 25 kHz, channel induced intersymbol interference is not a major concern in this design.

However, the rapid periodic fading caused by vehicle motion does constrain data rate, packet length, and required E_b/N_0. This fast Rayleigh fading is the major source of concern for this design. As the vehicle speed decreases, the average fade duration increases resulting in more bit errors per fade. At the same time the number of fades per second decreases. Together, these conditions imply a constant average bit error rate per block [6]. The (63,47) Reed-Solomon block error correction scheme that has been chosen can handle the

worst case burst errors as well as the overall average random error rate [7].

Fundamentally, there were two alternatives for the selection of modulation/demodulation. A noncoherent limiter-discriminator detection scheme could be used directly utilizing the direct FM modulator and limiter-discriminator already build into the radio. Alternatively, a double layer modulation scheme with an arbitrary modulation format residing on a new carrier residing in the center of the radio baseband input was considered. The direct FM scheme was chosen due the simplicity of implementation. Although almost any CPFSK modulation scheme could have been implemented, we chose Differential GMSK (DGMSK) due again to the ease of implementation and its relatively good tradeoff between spectral efficiency and bit error rate performance. Differential modulation and detection was required due the presence of radio repeaters in the overall system implementation. An odd number of spectral inversions of the baseband waveform could occur which reverses the sense of the data encoding (i.e. the received signal constellation is rotated 180 degrees causing any absolute encoding to be inverted).

The synchronization problem was limited to bit and frame. Overall packet transmission timing is controlled by an external host processor. A convolutional data scrambler/descrambler was implemented to ensure data bit transitions were independent of the actual data being sent. This guarantees that long strings of 1's or 0's do not have a deteriorating effect on the bit synchronization process.

Finally, the overall system requirement is that the mobile modem be half-duplex and the compatible fixed end modem be full-duplex.

III. Hardware Architecture

- Design goal to keep the circuit card under 22 square inches for economical manufacturing
- Minimizing total parts count and cost
- Accept 9 - 32 VDC inputs with low voltage and transient protection to vehicular standards
- Support over-the-air communications at rates of up to 8000 bps
- Power consumption <200 mA at +12 VDC, nominal
- -40°C to +85°C operating temperature range

A DSP-based architecture was chosen because it provided the greatest flexibility in designing the modem and allowed the most freedom to cost reduce the unit. The basic hardware platform is built on a 5.5" X 4", 4-layer printed circuit card. It consists of 26 ICs, one oscillator and one crystal. The nominal power consumption is 2.5 watts.

The Texas Instruments TMS320C5x DSP processor family was chosen for its low unit price, its high performance (20MIPS), small footprint, good firmware development tools along with additional family members to increase performance when necessary. There are five external interrupts; four general purpose, prioritized interrupts and one non-maskable interrupt.

Main memory consists of 64KBytes of zero wait state SRAM. It is used for both program execution and data base storage. In addition, 64KBytes of EEPROM provides for program storage. This EEPROM can be field programmed through the unit's communication ports. An optional 64KBytes of one wait state SRAM is also provided for future expansion. 32, 16-bit words of non-volatile RAM are included with automatic EEPROM restore and backup every power cycle. This serial NVRAM is used for variable and statistics storage. The EEPROM portion may be accessed over 1,000,000 times with over 100,000 writes.

Communication with external devices and programming of the on-board EEPROM is done using two serial ports. Each serial port is independently configurable for either RS-232 or direct, single-ended 5 V CMOS level communications. Both ports may be optionally ESD protected to over 10 kV.

As a companion to the TMS320C5x processor, the TMS320AC01 14-bit synchronous linear CODEC was chosen to perform the A/D and D/A data processing functions of the data to/from the radio's audio ports. This CODEC has a conversion rate of up to 43.2 kHz with internal pre- and post scaling amplifiers to set the signal levels. The sampling rate is continuously variable from external control and is used as part of the overall modem bit synchronization loop. However, the inability to independently control the input and output sampling rates restricts the modem operation to half-duplex. The CODEC also includes a complete set of anti-aliasing and reconstruction filters. Two electrically adjustable and programmable potentiometers are used for calibrating the modem when ultimately connected to a radio. This allows these levels to be adjusted without violating the integrity of the unit housing the modem. Differential to single-ended and single-ended to differential conversion circuitry is supplied for interfacing to the radio. This circuitry also provides additional filtering and level adjustments, allowing the CODEC to be mated to different radio platforms and input/output interface level, impedance and drive requirements.

There are 24 parallel I/O lines; 16 output and 8 input. There are 6 LEDs used for displaying system and communications status. All communications and power

to the unit is done through a standard 34-pin, 0.100" center locking ribbon connector. All I/O lines going to external unit pins may be fully protected against ESD and shorts to ground or to the input voltage level without suffering permanent damage.

The buck configured switching power supply can produce up to 4.5 watts at 5 VDC +/- 3% with no heat sinking required. Additionally, the power supply is designed to CROWBAR with 500 millisecond transients over 44 VDC.

Referring back to the overall system design, the fixed-end version of the modem is required to be full - duplex. This is accomplished by architecting two mobile modems in a master/slave relationship, with the transmit-only unit being the master. The connection between the two simplex modems was done using Texas Instrument's high speed interprocessor TDM serial communications link. The mobile modem TMS320C52 processor was exchanged for a TMS320C51 which provides this additional built-in capability. The link operates at 5 Mbps. By changing the only the processor, one oscillator component, and providing a number of selectable configuration jumpers, over 99% of the modem unit can be reconfigured for the fixed station application.

IV. Software Architecture

Implementing both the control and signal processing functions of the modem on a single CPU requires that careful attention be given to managing the CPU and the context in which various tasks execute. Merging signal processing and control functions on a single DSP CPU can be managed by a real-time kernel that segregates high-priority, synchronous signal processing functions from lower-priority, asynchronous, control functions.

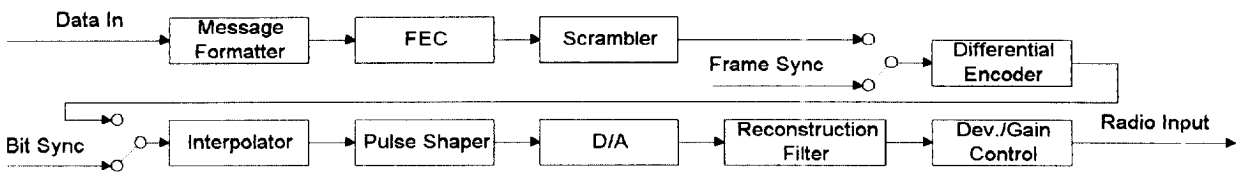
Traditional signal processing algorithms typically involve short sequences of code, with a linear execution path, executed synchronously on input and output data streams at a rapid rate (20 kHz or higher). The code for these algorithms is usually written in assembly language. Control functions and baseband processing, however, are more complex, both in structure and control flow, and execute at a much slower rate, typically on a packet-by-packet basis, or about 10 - 20 Hz. Also, the control and processing functions may execute asynchronously with respect to the incoming or outgoing data stream. These functions are often written in a high-level language such as 'C' to improve reliability and shorten development time. A key requirement in the design of the underlying operating system is that both high rate, synchronous, uncomplicated processes and lower rate, asynchronous, complex processes be supported efficiently.

The system kernel developed for the modem is a hybrid, real-time task-switching kernel. It supports both preemptive and non-preemptive task switching, concurrently. After examining commercially-available alternatives, the decision was made to develop the kernel in-house so that it could be optimized for the task of supporting the modem functionality. The signal processing tasks are initiated preemptively, requiring a software context switch. Since the signal processing tasks are by nature synchronous, the need to process signals (semaphores, event flags, etc.) is non-existent, and the context switch to the signal processing tasks can be made very efficient. The control tasks, which operate asynchronously, require more traditional real-time O/S support in terms of signals and messages that can be posted between tasks. Task-switching between control tasks is non-preemptive. This has the advantage of improving the determinism and testability of fundamentally asynchronous, event-driven tasks, and allows the context switching process to be simplified.

Transmit Side Processing

The transmit side functional block diagram is shown in Figure 1. As this modem is expected to find use in applications with an abundance of short GPS position messages, the over-the-air protocol was designed to handle short messages efficiently and longer messages flexibly. To transmit a message, the modem outputs a bit sync pattern of alternating 1's and 0's. This is followed by an 80-bit frame sync pattern of repeating Barker codes. It achieves better than 10^{-6} probability of false detect against a BER of 0.25 (20 bit burst errors). The frame sync is then followed by one or more message blocks consisting of message data and Reed-Solomon parity.

Figure 1. Transmit Functional Operation



Short messages require only one message block. Longer messages require multiple blocks; the first block contains additional message framing information. To make it possible to decode one-block messages, some message framing information is embedded in the frame sync pattern. That way, the modem firmware can tell before the first block is decoded if a message comprises multiple blocks or just the one. This is necessary since when there are multiple blocks, the initial block (with message framing information) will finally be decoded by the Reed-Solomon processing routines 15 to 30 milliseconds following the start of the second block.

Following the FEC, bit sync, and frame sync headers, the data is differentially encoded by a simple running exclusive-or operation. Each transmitted symbol is represented by 4 data samples, i.e. 4 samples/baud. This is achieved by interpolating 3 zero-valued samples between each transmitted data sample. This sample sequence is then convolved with a Gaussian pulse shaping filter. A pulse shape corresponding to a BT=.3 was chosen. This filtered sequence is processed by the D/A converter within the CODEC, filtered, and passed to the analog radio input processing circuitry described earlier.

Receive Side Processing

The receive side processing is basically the dual of the transmit side. The analog input to the modem is a gain adjusted version of the radio limiter-discriminator output. An anti-aliasing filter is provided by the CODEC prior to the A/D conversion. A digital FIR matched filter is implemented with a Gaussian impulse response and a BT=1.0. The A/D sampling rate is controlled by a simple first order tracking loop [8]. The output of the A/D is passed directly to the DSP and an absolute value nonlinearity. The output of this nonlinearity is multiplied by the sequence generated by the CODEC's internal NCO. The resulting error sequence is processed by the first order loop filter and used to drive the NCO frequency.

The slicer or bit threshold detector is a two-level variation of the multilevel scheme used in [4]. The Reed-Solomon decoder follows the differential decoder and frame sync algorithms.

The complexity of implementing forward error correction (FEC) is one the main reasons for the physical segregation of control and DSP processes in other modem designs. Some preliminary analysis and measurements were performed to determine the feasibility of integrating DSP functions and high-level processes on the TMS320C52 CPU. The forward error correction (FEC) employed is a traditional Reed-Solomon (63, k) implementation, coded in 'C', using Berlekamp's algorithm to determine the error polynomial $\sigma(\mathbf{X})$ and a Chien search to identify the roots (error locations) of $\sigma(\mathbf{X})$ [8]. The symbol size is fixed, at 6 bits, but k (the message size) can be changed on a message-by-message basis, by using a shortened code. In addition, the strength of the generated parity t (the number of correctable symbols) can be adjusted to optimize message length for a particular data link. One feature of the implementation of Berlekamp's algorithm is that its memory requirements are independent of the values of k and t.

The throughput achieved by the Reed-Solomon algorithm on a TMS320C52 CPU running at 20 MHz is an important system consideration. In the following summary, m is the number of bits per symbol, k is the size of the message (in symbols) and t is the number of correctable symbols (the number of parity symbols added to the message by the Reed-Solomon algorithm is $2t$).

The application-dependent message size was 16 symbols (12 bytes). The delay of the decoding algorithm grows non-linearly over t, mostly as a function of t^2. By taking into account the rate at which the delay grows for various parts of the algorithm, making some approximations and measuring several actual delays, the processing delay can be empirically estimated as a function of t by $(3/52)t^2 + t$. Delays for other values of t can then be calculated to within a few percent.

$m = 6, k = 16$

t:	6	7	**8**	9	10	**11**	12	13	14
delay (ms):	**8.2**	10	**12.0**	14	16	**18.7**	21	24	27
throughput (K bits/sec)	**20.5**	18	**16**	14.6	13.5	**12.2**	11.4	10.5	9.8

Table 1. Reed-Solomon throughput analysis

Our assumption was that 50% of the CPU cycles in a modem implementation would be available for performing Reed-Solomon calculations, implying that a worst-case 5 Kbps data rate can be supported up to about the level of t=14. In practice, the presence of bit and frame sync sequences, as well as the occasional longer messages, allow even stronger levels of FEC to be applied and decoded "on the fly" (without pre-encoding messages).

Increasing m (the number of bits per symbol) affects only the delay associated with Chien search algorithm, which represents about 25% of the total processing budget when m = 6. The Chien search algorithm delay increases (approximately) as 2^m. For m = 7, this is a total increase of approximately 25% over m = 6. If m is increased to 8, then for a given t the delay is approximately 75% larger.

For a fixed block size containing $m \times k$ message bits and $m \times 2t$ parity bits, the delay required to decode the block is fairly constant over m (at least for larger values of t). Since smaller symbol sizes are more efficient in terms of other processor resources (look-up tables, etc.), this implies that the smallest symbol size which can be used to support the required maximum block length and level of FEC should be used.

Following the FEC the resulting data sequence is descrambled and appropriately formatted.

VI. Modem Performance

All of the basic modem algorithms were simulated either in "C" on a 486-based PC or on the Comdisco Systems Signal Processing Workstation (SPW) on a SUN Unix platform. The digital shaping filters were generated using a MOMENTA digital filter design package.

Final system BER testing was done at RF using a custom noise source and a Hewlett-Packard 11759B RF Channel Simulator at RF frequencies of 450 MHz and 900 MHz. Motorola SPECTRA land mobile radios were used at both the mobile and fixed end. A spectrum analyzer was used to set E_b/N_0. The modem tested operated at a sampling rate of 20 kHz and a symbol rate of 5 kbaud. The radiated power spectrum fully conforms to FCC Part 90.209.

BER Performance was measured at E_b/N_0 from 16 to 63 dB under both AWGN only and AWGN plus Rayleigh fading from vehicle motion of 10 to 40 km/h. With AWGN only, the modem is about 3 dB worse than theoretical for a two-level non-coherent detector [2]. This corresponds to a 10^{-3} BER at 18 dB E_b/N_0 and 10^{-6} BER at 21.5 dB. At 40 kmph, the modem requires 43 dB E_b/N_0 for 10^{-3} BER and reaches an irreducible error rate of 3.0 x 10^{-5} BER at 58 dB E_b/N_0. This performance is consistent with both published theoretical results [5] and empirically derived measurements of competitive products.

VII. Conclusion

In summary, all design requirements were met or exceeded. This development has demonstrated that a very low cost single DSP processor solution for the control and real time processing required by VHF/UHF land mobile radio modems is achievable.

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