A Neural Analog-to-Digital Converter with Resolution Enhancement

D. A. Comisky, J. M. Drake, and G. L. Dempsey
Electrical & Computer Engineering & Technology
Bradley University
Peoria, Illinois 61625

Abstract

A neural-based analog-to-digital (A/D) converter was first proposed by Tank and Hopfield in 1986. Hopfield applications have typically used high-gain amplifiers for the neurons. Unfortunately, this led to missing output codes and unequal step widths in the A/D converter application. The new approach proposed here use low-gain analog amplifiers for the artificial neurons. This allows additional bits of information to be extracted from the A/D converter output. In this paper, we discuss the hardware implementation of our resolution enhancement method applied to a four-bit neural A/D converter. The method yielded an increase in resolution from 4 to 8 bits.

1 Introduction

An analog-to-digital (A/D) converter's resolution is dictated by the number of A/D bits (n) in conventional approaches. A n-bit A/D converter is limited to 2^n output codes. A neural-based A/D offers the possibility of improving resolution (increasing output codes) without a significant increase in hardware. This can best be illustrated by observing the input-output characteristic of the Hopfield neuron shown in Fig. 1. The significance of this smooth curve (a sigmoid) is that it illustrates that the output has an infinite number of states as opposed to digital methods which have two states (logic "1" or logic "0"). The function of a resolution enhancement method is to extract this additional information.

The neural A/D approach has received attention [1-4] since it was initially proposed by Tank and Hopfield [5]. The previous methods have used or assumed that the neurons were either digital or very high-gain analog amplifiers. Our method uses analog amplifiers for the artificial neurons with gains similar to their biological counterparts [6]. In this paper, we discuss the addition of a resolution enhancement method to a four-bit neural A/D converter. The hardware implementation of the discrete component circuit consisted of over fifty operational amplifiers (op-amps). Resolution was increased from four to eight bits (worst case) with a conversion time of less than one hundred microseconds.

2 A/D Converter with Low-Gain Neurons

Our neural A/D converter is based on the Tank and Hopfield 4-bit A/D network presented in [5]. The network was designed to convert analog voltages in the interval -0.5 to 15.5 with a conversion step of one volt. Each A/D bit requires one neuron. The neuron or amplifier using the Hopfield network topology is shown in Fig. 1. Only the inverted output is required for the A/D application. Our simulation of the Tank and Hopfield A/D is shown in Fig. 2 (analog input x versus digital word). The ideal switching points (changes in output codes) occur at integer multiples of 0.5 volts.

We have presented a new design strategy to eliminate the problems (missing output codes and unequal step widths) associated with the Tank and Hopfield A/D converter [6]. The experimental results of this new method is shown in Fig. 3, which indicates approximately equal step widths. The improvements are due to the development of a modified Hopfield neuron, which allowed a gain reduction from 160 to 16 [6,7].

Figure 4 shows a block diagram of the modified neuron. The first stage is an inverting summing amplifier. The second stage provides the neuron gain and bounds the output at 0 volts (logic "0") and -1 volt (logic "1"). The input-output voltage relationship for the neuron in the linear region of operation is

$$V_i = G\,u_i \qquad (1)$$

where G is the neuron gain or slope of the input-output characteristic shown in Fig. 4. The nonlinear differential equation describing each neuron i is

$$C_i(du_i/dt) = -u_i/p_i + I_i + \sum_{\substack{j=0 \\ j\neq i}}^{n-1} T_{ij}\,V_j \qquad (2)$$

where n is the number of neurons, u_i is the input voltage of the neuron, I_i is the input current, C_i is the input capacitance, the T_{ij}'s are the synaptic weights, and p_i is

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the neuron cell input resistance.

A block diagram of our A/D converter without resolution enhancement is shown in Fig. 5. The energy function of our network is

$$E = -0.5 \sum_{\substack{i=0 \\ i \neq j}}^{3} \sum_{j=0}^{3} V_i V_j T_{ij} - \sum_{i=0}^{3} I_i V_i + 0.5 \sum_{i=0}^{3} \frac{V_i^2}{p_i G_i} \quad (3)$$

where

$$T_{ij} = (-2^{(i+j)})/32 \quad (4)$$

and

$$I_i = (-2^{(2i-1)} + 2^i x)/32 \quad (5)$$

Each neuron output is connected to the other neurons through a conductance T_{ij} of $2^{i+j}/32$. The input current described in (5) consist of two terms. The first term corresponds to a reference voltage of -1 volt (the conversion step size) which is connected to each neuron through a conductance of $2^{(2i-1)}/32$. The second term in (5) corresponds to the analog input voltage x, which is connected to each neuron through a conductance of $2^i/32$. A R-2R ladder network was used to create the resistance ratios in (4) and (5).

The objective of the network is to converge to a solution such that the neural output (V_3, V_2, V_1, V_0) is approximately equal to the digital representation of the analog input voltage x, which can be expressed analytically as

$$\textit{neural output} = \sum_{i=0}^{3} V_i 2^i \approx x \quad (6)$$

3 Resolution Enhancement Method

The key to resolution enhancement for the neural A/D is using low-gain neurons. Because of the low gain, our network outputs are analog voltages instead of digital logic levels. Of course, these analog outputs contain valuable information in the A/D application. Extracting this additional information will result in an improvement in the A/D's resolution. As an example, for an input voltage of 7.5 volts, our network outputs (V_3, V_2, V_1, V_0) are equal to -0.5 volts, or halfway between logic "0" (0 volts) and logic "1" (-1 volts). Substituting these values into (6) yields the exact answer, i.e., output equals input. Similar results are obtained at the other switchpoints (integer multiples of 0.5 volts).

A block diagram of the resolution enhancement method implemented in hardware is shown in Fig. 6. An Intel Corporation 8751 microcontroller was used to perform the network reset, sample/hold control and timing, and the resolution enhancement. Extracting the additional bits of information from the 4-bit neural A/D converter was accomplished by perturbing the converged value of the least significant bit (LSB) neuron's output. A neuron gain of 16 was selected to guarantee the LSB neuron output remains in the linear region of operation for all input voltages. A more accurate solution can be computed by knowing the amount of perturbation voltage required to produce a new logic state output (defined in next section) for the LSB neuron. The accuracy with which this can be performed is dependent on the perturbation method and associated hardware limitations. The perturbation signal is applied only to the LSB neuron output after convergence. An 8-bit digital-to-analog (D/A) converter was used to generate the perturbation signal.

3.1 Hardware Description

The circuit implementation of the LSB neuron without resolution enhancement is shown in Fig. 7. The first stage is a summing amplifier with a gain of one. The feedback voltages from the other three neurons, the -1/64 volt reference, and the analog input voltage x/32 are derived from R-2R ladders as dictated by (4,5) and applied to the summing stage. The second stage sets the neuron gain to 16. The precision limiter circuit consisting of three op-amps restricts the neuron output at -1 volts minimum and 0 volts maximum.

The neuron time constant stage filters the precision limiter output before it is applied to the R-2R ladder. Conversion time for the neural network is a function of the analog input x and is significantly slower near the switchpoints. To combat this problem, a faster time constant is switched in for the LSB and LSB+1 neurons after an appropriate delay (after MSB and MSB+1 neurons have converged).

The analog switch between the first and second stage is used for the reset operation, which is critical for equal step widths. Each neuron output is converted to a digital value using a separate comparator with a threshold of -0.5 volts. Voltages less than -0.5 volts are defined as logic "1", voltages greater than 0.5 volts are defined as logic "0". Even though comparators (high-gain amplifiers) are used here, the neural decision has been made with low-gain amplifiers.

The modifications added to the LSB neuron for resolution enhancement are shown in Fig. 8. A sample/hold device is used to maintain the LSB neuron's output level from the gain stage while the resolution enhancement is administered. As shown in the figure, the comparator output is now dependent on the summation of the LSB neuron output and the perturbation signal generated from the 8-bit D/A converter via the microcontroller. The number of D/A bits dictates the overall

accuracy of the resolution enhancement. For example, the maximum possible resolution for this hardware implementation is 12 bits, 4 bits from the neural network and 8 bits of resolution enhancement. Unfortunately, other factors such as system noise levels, component tolerances and nonideal op-amp characteristics, also limit the resolution. With a discrete component circuit consisting of off-the-shelf components, we achieved 8 bits of resolution worst case (4 bits from neural network, 4 bits of resolution enhancement). The A/D input-output characteristic is shown in Fig. 9.

Figure 10 shows the convergence of the four neuron output voltages with an input voltage of 2.1985 volts. The worst case convergence time of the neural network was 16 microseconds but was typically less than 5 microseconds. The total conversion time with resolution enhancement was 96 microseconds where 75 percent of this time is attributed to the software computations.

3.2 Software Description

A description of the resolution enhancement software is shown below. The extra bits of resolution are obtained using a successive approximation algorithm. The neural network switchpoints were obtained experimentally and stored in the microcontroller's RAM memory. This compensates for the majority of the nonideal op-amp characteristics.

Resolution Enhancement Software

1. Power up: Perform neural network reset.
2. Release reset and allow neurons to converge.
3. After 5us delay, switch in fast time constants.
4. Delay 10us to allow for neural convergence.
5. Read neural network 4-bit output. The LSB neuron's gain stage output is latched with sample/hold device.
6. The 4-bit digital output is evaluated. The LSB determines the course of action for the successive approximation method. Each step or cycle in the successive approximation requires 2 or 3us to complete depending on the LSB voltage. The network is reset during the resolution enhancement to minimize conversion time.
7. The 12-bit output voltage is computed by adding or subtracting the perturbation voltage from the appropriate switchpoint stored in RAM memory.
8. The 12-bit output is written to a 12-bit D/A converter for instrumentation purposes.
9. The cycle is repeated (Go to step 2).

The successive approximation method is shown in Fig. 11. The upper trace is the LSB neuron output before the sample/hold device. The lower trace is the summation of the LSB output and the perturbation signal generated by the D/A converter. At the fourth tick on the graph, a successive approximation sequence has been initiated. The sequence converges to the -0.5 volt level where the perturbation voltage is then added or subtracted to the appropriate switchpoint stored in RAM memory. The calculated output is written to a 12-bit D/A converter. This D/A converter was used to display the input-output characteristic shown in Fig. 9.

3.3 Improvements

Although other hardware schemes were considered, it was felt that the microcontroller would be more flexible for the first iteration of the resolution enhancement method. Approximately 75 percent of the conversion time was attributed to software computations. A 12MHz microcontroller with a maximum instruction cycle time of 2 microseconds was used for the implementation. Conversion time can be decreased with the 48Mhz version of the microcontroller.

A VLSI implementation can offer further improvements in resolution enhancement and a reduction in conversion time. Laser trimming techniques can be used for critical components such as the R-2R ladders. The successive approximation algorithm can be implemented with logic circuitry, which eliminates the software execution time.

Acknowledgments

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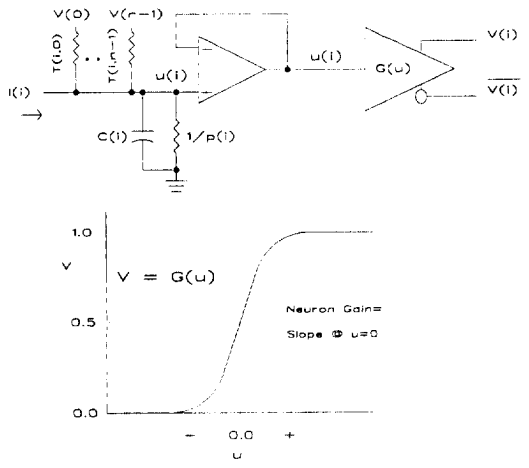

Fig. 1. Hopfield Neuron Model.

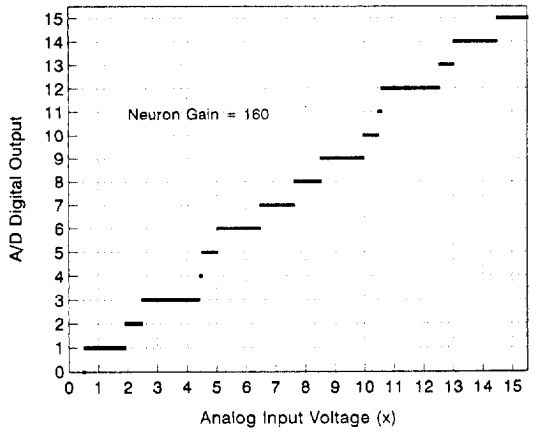

Fig. 2. Tank and Hopfield A/D Input/Output Characteristic (simulation).

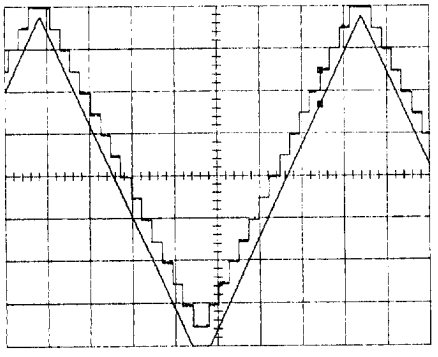

Fig. 3. Modified A/D Input/Output Characteristic (experimental). Triangular wave corresponds to the input voltage (lower trace). Staircase waveform corresponds to neural output (upper trace). Triangular wave input frequency is 2.65 Hertz.

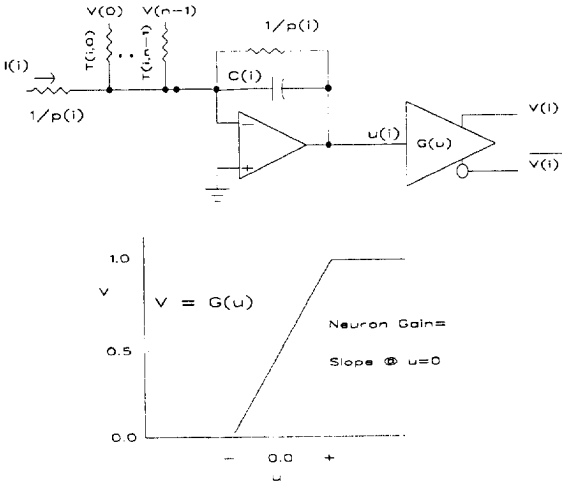

Fig. 4. Modified Hopfield Neuron Model.

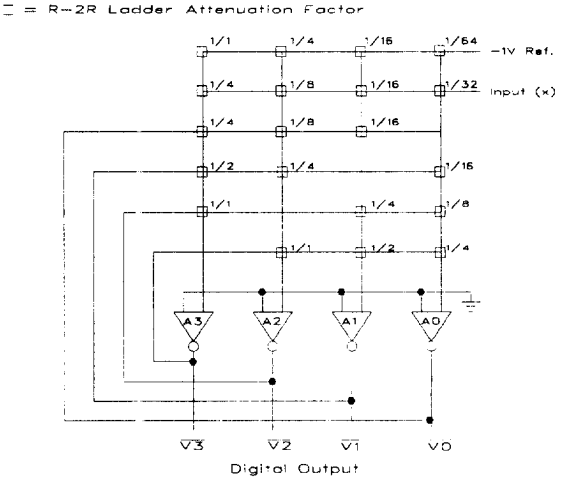

Fig. 5. Modified 4-bit A/D Network.

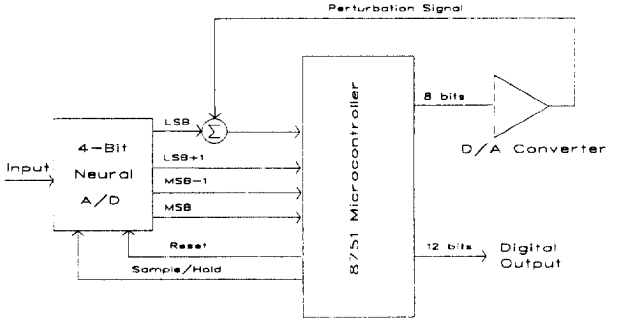

Fig. 6. Resolution Enhancement Hardware Topology.

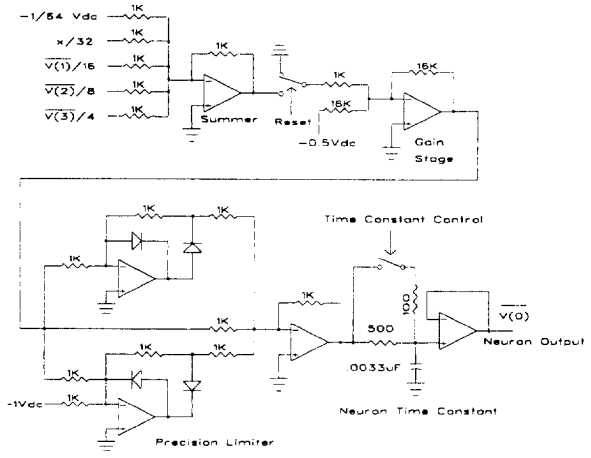

Fig. 7. LSB Neuron Circuit Implementation.

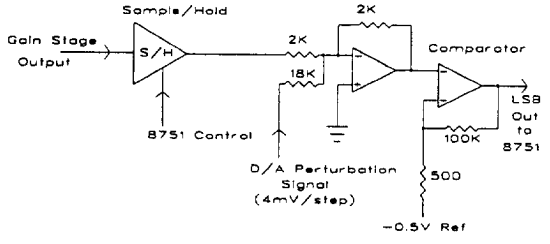

Fig. 8. LSB Neuron Circuit Implementation for Resolution Enhancement.

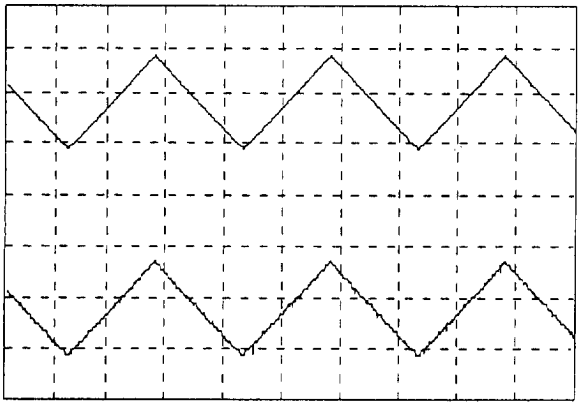

Fig. 9. A/D Input-Output Characteristic with Resolution Enhancement. Vertical scale is 5 volts/ division. Horizontal scale is 100 ms/division. Triangular wave input frequency is 3.3 Hertz (upper trace). Lower trace is resolution enhancement output.

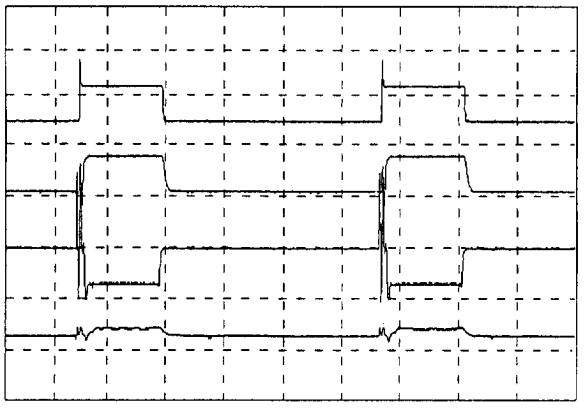

Fig. 10. Analog-to-Digital Converter Neuron Outputs. Vertical scale is 0.5 volts/division. Horizontal scale is 20 us/division. The initial outputs are equal to -0.5 volts before application of input x of 2.1985 volts. Top trace is MSB neuron, bottom trace LSB neuron.

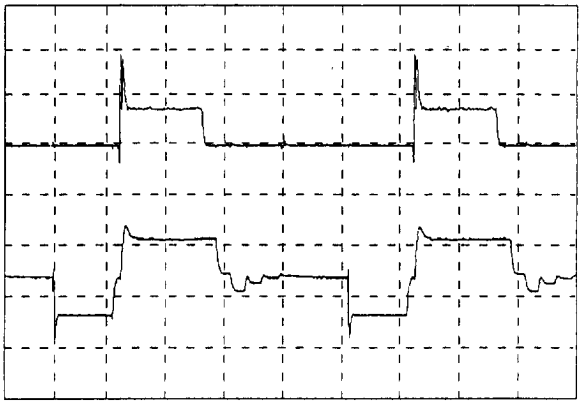

Fig 11. Resolution Enhancement by Successive Approximation. Upper trace is LSB neuron's analog output voltage. Lower trace is the summation of the LSB output and the perturbation signal. The successive approximation sequence is started at the fourth vertical tick. Vertical scale is 0.5 volts/div. Horizontal scale is 20us/div. The analog input voltage x is 2.9140 volts.