On Behavioral Modeling of Analog and Mixed-Signal Circuits*

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Abstract

Behavioral simulation of complex, inherently highly nonlinear mixed-signal systems is often the only effective way to evaluate possible system performance before fabrication and characterization of the hardware system. Transistor-level, SPICE, simulations of these systems are often practically impossible because of the enormous computational time required due to the many interactions of all the nonlinearities and the widely separated system time constants. New behavioral models for useful electronic functions have been developed as straightforward mathematical descriptions that can be evaluated by general purpose mathematical programs and system simulators. Our models are targeted for MATLAB and use standard MATLAB expressions and linked C and FORTRAN codes. An example PLL behavioral model is presented and evaluated by comparing simulated performance to actual experimental integrated circuit performance.

Introduction

For many complex analog and mixed analog/digital systems, computer simulation at the nonlinear device level is not practical due to the computational time involved. Given that the complexity of system integration will only continue to increase, simulation of the expected system performance is and will continue to be a critical issue in circuit development. In many analog design situations it would also be advantageous to efficiently simulate an analog system at a higher level of abstraction and compare several different realizations before undertaking the final IC design. As an alternative to very expensive and time consuming nonlinear device-level simulation, more efficient "behavioral simulation" is becoming more acceptable. Behavioral simulation uses "behavioral models" that reflect the terminal characteristics of functions realized by circuits rather than the transistor-level details of the circuits. Most "behavioral models" are SPICE sub-circuit "macromodels" (see, for example [1-4]). Some are designed for true behavioral simulators that may use unusual specification languages or input formats [see, for example, [5-8]). Behavioral simulation CAD tools require behavioral models that must be developed with a balance of computational efficiency and performance accuracy. The behavioral model must accurately represent the electronic function's overall performance; not only the nominal idealized performance but also the limitations of performance. Our behavioral models are designed for use in MATLAB and as such use straightforward mathematical descriptions of the functions that may be coupled with FORTRAN or C codes, if necessary. We have created a library of new efficient behavioral models for analog functions that are part of a new computer aided design (CAD) tool that we are developing to assist in the fast prototyping of analog CMOS ICs [9]. Each behavioral model provides an accurate representation of the nonlinear, time-domain terminal characteristics of its analog function. Each behavioral model also provides a computationally efficient simulation that includes performance limiting characteristics. Some of our new behavioral models provide simulations that are as much as 2 orders of magnitude less computationally expensive than full nonlinear device simulation with SPICE. The overall CAD system that uses these behavioral models was described in [9]. In [9], example behavioral models were briefly described as an essential part of the overall CAD system and the accuracy of a model's behavior was shown to support the claimed utility of the overall CAD system. In this paper, a new behavioral model for a more complex function (that contains both analog and digital sub-functions) is presented and its accuracy demonstrated by comparisons of model and experimental IC performances. As an example, the mixed-signal charge pump phase/frequency-locked-loop behavioral model illustrates the power, versatility, and efficiency of this approach to analog circuit simulation and design.

To allow the reader to put our behavioral model discussions in context, we now review the overall CAD system within which they function. This CAD tool that we are developing to assist in the fast prototyping of analog CMOS ICs [9] is based upon the availability of a library of pre-characterized functional blocks and allows the designer to create an analog circuit by selecting analog function blocks from the library and interconnecting them in a block-diagram-level design capture and simulation page. The new analog circuit is then simulated at a behavioral level to evaluate circuit performance. Using cell layouts from the cell library, the IC layout is then assembled by a cell placement and routing program. Each functional block in the library represents a behavioral model, a SPICE sub-circuit model extracted from the cell

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layout, and the cell layout. The behavioral model, SPICE sub-circuit, and experimental performance of the analog function cells are carefully reconciled to make the behavioral simulations as realistic as practically possible. Actual loading of each block is estimated from the block diagram and included in the behavioral simulation. The library of pre-characterized analog function cells we have developed is realized in the 2-micron p-well MOSIS process; however, libraries may be realized in any technology. Given adequately well behaviorally modeled analog function cells, the use of behavioral simulation in analog design should increase the efficiency of analog and mixed-signal IC creation.

In this paper, a new behavioral model for a mixed-signal phase/frequency-locked-loop is presented and its performance discussed. The model performance is compared with experimental performance data from the associated integrated circuit. The accuracy of this behavioral model is excellent and the computational cost of using the behavioral models can be as low as 2 orders of magnitude less than SPICE simulations.

Behavioral Model of a Mixed-Signal Phase-Locked-Loop

Phase-locked loops (PLLs) are versatile building blocks contained in many larger systems. For example, PLLs are useful for timing recovery, waveform synthesis and demodulation. This particular PLL is mixed-mode in that it consists of an analog voltage controlled oscillator (VCO) and loop filter, and a digital phase-detector. The circuit level schematics for each of these components are shown in Figures 1-3, respectively. The VCO consists of a wideband voltage-to-current (V-I) converter and a current-controlled relaxation oscillator. The two resistors, R1 and R2 in the V-I converter, and two identical capacitors in the relaxation oscillator set the VCO operating point and gain, Ko. The loop filter is of standard design with C1 used for surge suppression. The phase detector is a standard phase/frequency detector which has a tri-state "charge pump" for loop filter integration of the outputs of the digital latches or holding the last available state on the loop filter if the outputs are inactive. From theory, one can show that the gain (Kd) of the phase detector is (Vdd-Vss)/4π.

The primary design concern is that the PLL be as programmable as possible with respect to its large- and small-signal parameters. Due to the versatility of this particular PLL, a large amount of customization is left to the user. To this end, the behavioral model, shown in Figure 4, allows the user to choose as input the maximum and minimum free-running frequencies of the VCO (fmax and fmin), the loop damping coefficient (ζ), the loop natural frequency (ω_n) and the ratio C2/C1 (r) in the loop filter. Due to the programmability of the PLL, all resistor and resistor/capacitor time constants in the VCO and loop filter are in fact functions of these five parameters. The respective behavioral models for the VCO, phase detector and loop filter are now discussed in turn.

Analog Voltage Controlled Oscillator

The behavioral schematic for the VCO is shown in Figure 5. All behavioral models within our library have the ability to "look ahead" and adjust their capacitive and resistive loads based upon the models they are driving. The model of the VCO attempts to account for the important terminal behavior of the circuit without getting bogged down in the actual circuit level details. For instance, the oscillator is modeled by a two integrator positive feedback loop (at the top of the schematic in Figure 5) which produces a sinusoidal oscillation at a frequency determined by the output of the V-I converter model. The sinusoid is converted to a digital waveform via a simple clipping function preceding the VCO output. The operating point of the V-I converter is modeled as a sum of two currents which are functions of the user-defined frequency limits of the VCO. The minimum frequency of oscillation is used to program the offset current and thus sets the value of R2. The frequency range (fmax-fmin) is used to determine the gain of the VCO and thus sets R1 and C. The finite linear range of the VCO is modeled with a voltage saturation block in order to limit the incremental current which can be sourced to the oscillator. After summing the two currents due to R1 and R2, the value is passed to a function block which determines the instantaneous output frequency as a function of input current. The function models the delay around the relaxation oscillator loop to account for the non-linear current-to-frequency response for output frequencies roughly greater than 5MHz. Finally a frequency saturation block models the absolute maximum speed of the VCO. For this particular PLL, it is the VCO which limits the speed of the overall system.

Digital Phase Detector

The behavioral schematic for the phase detector is not shown as it is realized by some simple C code which implements the phase detector algorithm.

Passive Loop Filter

The behavioral schematic of the loop filter is shown in Figure 6. If C2/C1 is equivalent to r, the transfer characteristic of the filter may be written as: vcontrol/vin= $(1 + 2\zeta/\omega_n\, s)/(1 + (2\zeta\omega_n + k)/\omega_n^2\, s + 2\zeta k/(\omega^3(1+ r))\, s^2)$, where k is the loop gain, $K_o \cdot K_d$. Note that k may be extrapolated from the specification of the maximum and minimum free-running frequency for the VCO and the above specified gain for K_d. The VCO control voltage is derived from the above s-domain equation. The demodulated output, on C2, may be represented with a cascaded low-pass filter which contains a single pole at $\omega_n/2\zeta$.

Model Performance

In order to demonstrate the model's capabilities, a simple test setup shown in Figure 7 is used. The PLL functions as an FM demodulator with a VCO acting as the input source to the loop. It's frequency is modulated by a squarewave with frequency < ω_n. The small signal

response of the model may thus be obtained and three separate results are shown in Figures 8-10. I(n these figures, the first column (a) shows the behavioral model response of the loop, while column (b) shows the waveforms from oscilloscope measurements of an identical test setup. It can be seen that the behavioral model matches very closely with the actual measured results. However, PLL's exhibit a great deal of non-linear behavior over their operating range and the model's success at accounting for this is now demonstrated. If the input frequency jump exceeds the small-signal limits of the phase/frequency detector, a non-linear slewing is perceived on the VCO control voltage and the demodulated output. This effect is correctly predicted by the model and is shown in Figures 11-12. Another interesting study is that of the capacitor ratio r in the loop filter. By varying r, the steady-state control voltage jitter varies in its amplitude due to the surge suppression afforded by C1. Figures 13-14 demonstrate two identical loop setups for a capacitor ratio of 10 and 50.

Perhaps the most dramatic performance indicator of the PLL behavioral model is its speed of simulation. For example, this particular model is over 100 times faster than identical HSPICE simulations in obtaining the linear step responses of the PLL shown in Figures 6-8. This obviously allows the user to perform many more design iterations for loop optimization in the behavioral domain as compared to the HSPICE domain. In summary, the PLL behavioral model gives a great deal of insight into a complicated system's performance in a much quicker way than conventional SPICE testing.

Summary and Conclusion

Behavioral simulation CAD tools require behavioral models that must be developed with a balance of computational efficiency and performance accuracy. The behavioral model must accurately represent the electronic function's overall performance; not only the nominal idealized performance but also the limitations of performance. Our behavioral models are designed for use in MATLAB and as such use straightforward mathematical descriptions of the function that may be coupled with FORTRAN or C codes, if necessary. In this paper, a new behavioral model for a mixed-signal phase-locked-loop was presented and its performance discussed. The performance of this example PLL behavioral model is compared with experimental performance data from the corresponding PLL integrated circuit. The accuracy of the behavioral model is excellent and the computational cost of using the behavioral models can be over 2 orders of magnitude less than equivalent SPICE simulations.

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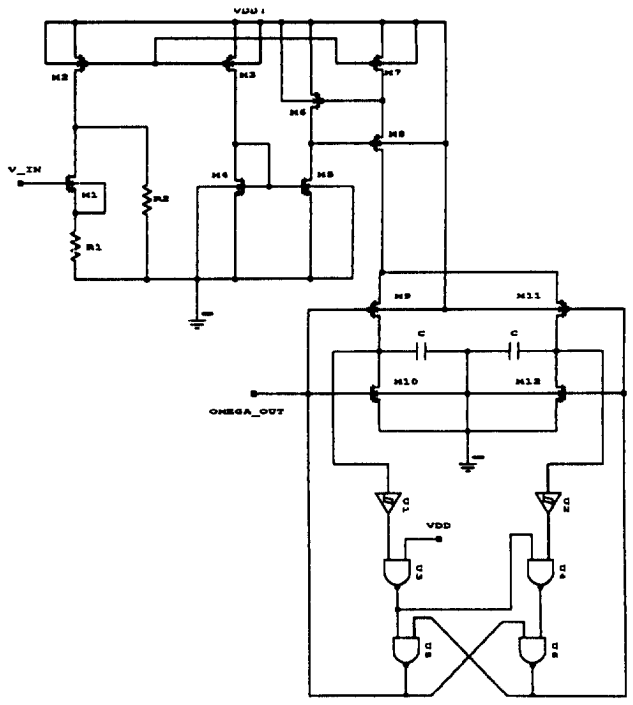

Figure 1 Schematic of voltage controlled oscillator

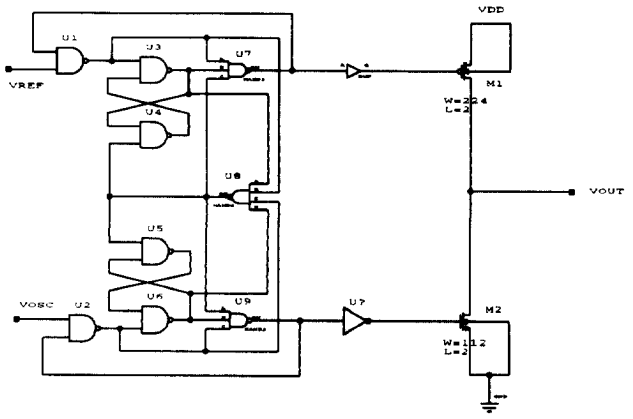

Figure 2 Schematic of phase/frequency detector

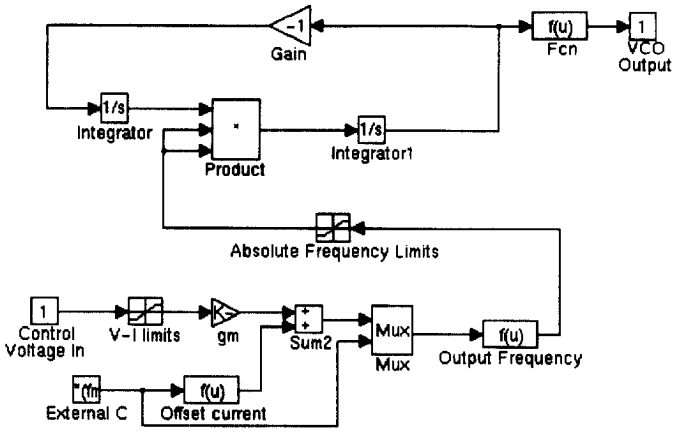

Figure 5 Block diagram of VCO behavioral model

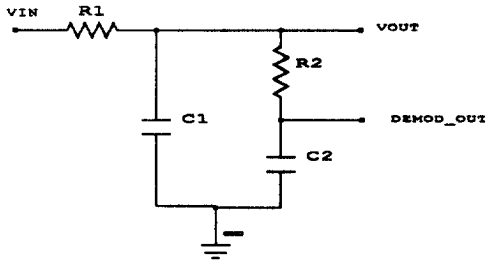

Figure 3 Schematic of loop filter

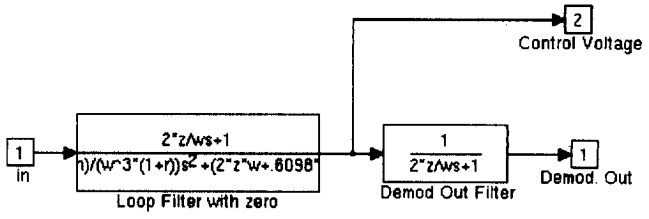

Figure 6 Block diagram of loop filter behavioral model

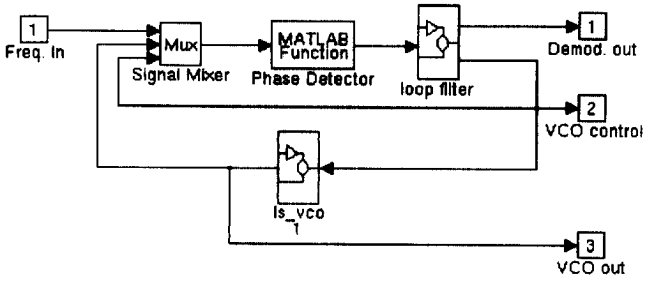

Figure 4 Block diagram of PLL behavioral model

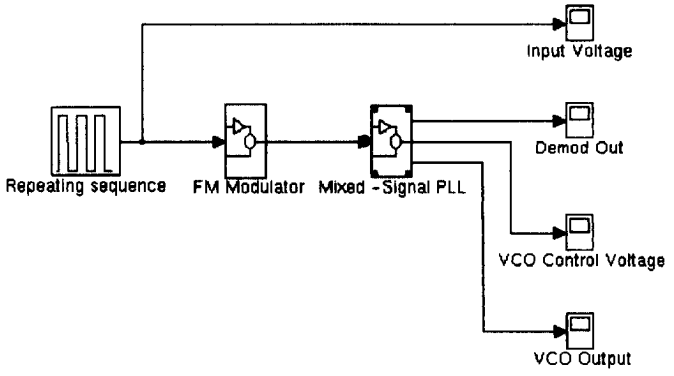

Figure 7 Block diagram of PLL simulation setup

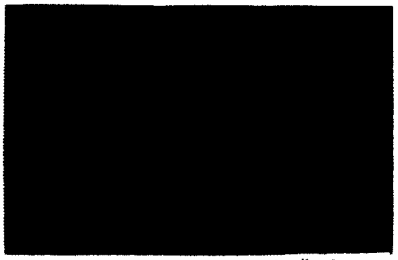

Figure 8a PLL step response for ζ=.5

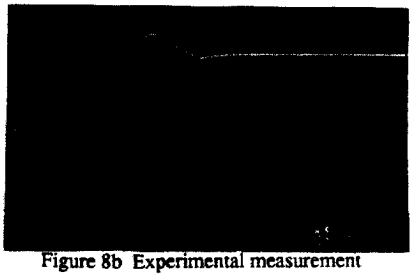

Figure 8b Experimental measurement

Figure 9a PLL step response for ζ=.707

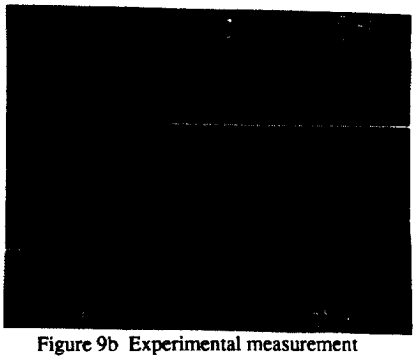

Figure 9b Experimental measurement

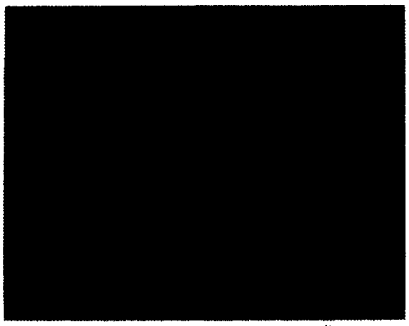

Figure 10a PLL step response for ζ=.85

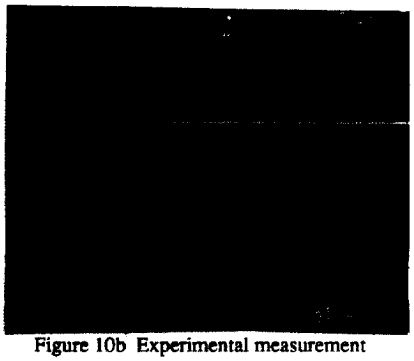

Figure 10b Experimental measurement

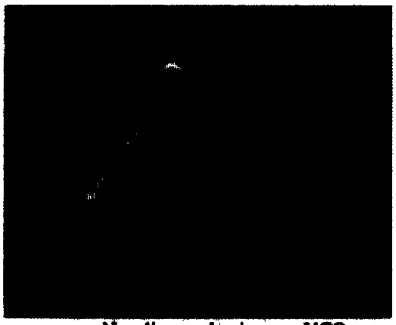

Figure 11 Non-linear slewing on VCO control voltage

Figure 12: Non-linear slewing on demodulated PLL output

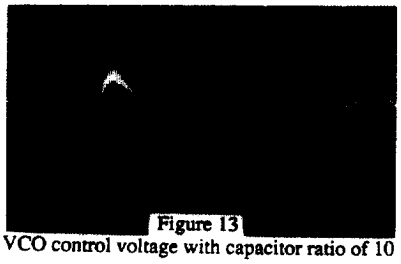

Figure 13
VCO control voltage with capacitor ratio of 10

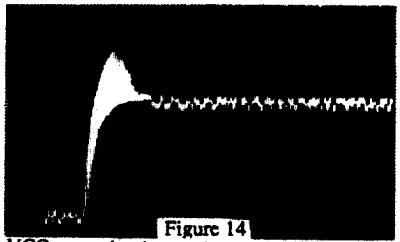

Figure 14
VCO control voltage with capacitor ratio of 50