An Analog Discrete-Time Transversal Filter in 2.0 \( \mu \text{m} \) CMOS

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Abstract

Analog discrete-time transversal filters can be implemented using track-and-holds (T/H's) as delay elements. With a classic linear tapped-delay line topology, the sampling rate is typically limited by the acquisition time of the T/H's. To overcome this limitation, a circular architecture was developed. The chip presented here is the first demonstration of the circular architecture. A four-tap equalizer has been fabricated in a 2 \( \mu \text{m} \) CMOS process, dissipates 148 mW when running at 30 MHz, and has a total area of 4.8 sq. mm.

1. Introduction

The density of a disc drive can be increased by increasing the linear density, or the track density. In either case, the SNR will be reduced due to intersymbol interference (ISI) and/or intertrack interference. Sampling detectors are an attractive alternative to the standard continuous-time pulse slimming filter and peak detector used in almost all drives today. The decision-feedback equalizer (DFE) and partial-response maximum-likelihood (PRML) detection using the Viterbi algorithm (VA) are the two most popular approaches. The DFE uses a standard linear equalizer (LE) as a forward filter to remove pre-cursor ISI, but then uses noiseless past decisions to cancel the remaining post-cursor ISI without the noise gain of a LE [1]. The PRML/VA detector uses sequence detection to improve on the bit error rate (BER) of bit-by-bit detectors [2]. For both DFE and PRML/VA detectors, the net gain over a continuous-time peak detect channel is that the desired BER can be achieved at a lower SNR, thereby allowing the density of the drive to be increased. Recent work shows that the density can be increased by 30-50% using current techniques [3], although more sophisticated sampling detection algorithms may achieve greater improvements in the future.

Both the DFE and the PRML/VA approaches require a LE, and the performance will be improved if this filter can be adaptive. The filter described here is intended to fill this need and is a part of a larger effort to develop analog implementations of sampling detectors for magnetic recording [4]. Although analog implementations require greater initial effort to develop, in a high-volume market like disc drives, the added cost can reasonably be amortized and the potential benefits of an analog approach make it worthwhile to pursue. Since the signal processing algorithms considered are relatively simple and don't require extreme precision (6 bits is usually enough), an analog approach can often be simpler and use less power than a digital approach. For example, the power consumption and cost of a high-speed flash analog-to-digital converter is significant, and is unnecessary with an analog approach. Also, analog multipliers, as might be used in the adaptive filters and in the detectors, are significantly smaller and lower power than their digital counterparts. In addition, analog solutions will typically be faster in a given technology.

Continuous-time analog [5-7], discrete-time analog, and digital filters can all be used as the equalizer in a disc drive read channel. However, because the equalization requirements change on different tracks of the disk, an adaptive filter, or at least a filter whose tap weights can be preloaded, is preferable. Since finite impulse response (FIR) transversal filters are guaranteed to be stable and can be made adaptive using well-known algorithms, they are an attractive approach. This paper deals with a discrete-time analog FIR filter, although continuous-time analog FIR filters are also possible.

An analog discrete-time FIR filter may be built from a serial arrangement of master/slave T/H's as shown in Figure 1. The held samples are multiplied by weights and added together to form the filtered output. The tap weights are digital because we have used multiplying digital-to-analog converters (MDAC's) in this first-generation design, but further benefits may be gained by using analog weights and full analog multipliers; we are currently investigating this option. The serial FIR architecture suffers for two reasons: (1) Each T/H must be a master/slave T/H (or else the memory of the delay line is wiped out when all of the T/H's go into track mode), which doubles the number of T/H's and doubles the clock frequency at which they operate, and (2) every T/H must acquire a new signal every clock period. The speed of an open-loop T/H is usually limited by how fast it can acquire its input signal.
after being switched from "hold" mode to "track" mode [8].
We propose a circular tapped-delay line architecture that
eliminates the need for master/slave T/H's and allows for
an arbitrarily long acquisition time of the T/H's.

Figure 1  Serial analog FIR filter architecture

Section 2 gives an overview of the circular FIR
architecture and its advantages and problems. Section 3
describes the circuits used in the chip design, Section 4
gives the measurement results from the chip, and conclu-
sions are stated in Section 5.

2. A Circular Tapped-Delay Line

Figure 2 shows the architecture for a four-tap equalizer,
utilizing two extra T/H blocks to increase the acquisition
time allowed. At any given time, four T/H's are holding
and two are tracking. At each positive clock edge, the T/H
that has been acquiring the longest is switched to hold
mode, and the T/H that has been in hold mode the longest
is switched to track mode. The T/H's can be thought of as
rotating counter-clockwise in the figure so that the newest
sample is fed into the multiplier with the weight for the
first tap. The time allowed for each T/H to acquire the
input signal is equal to the number of extra T/H's times
the clock period (in this case, two periods).

This arrangement will require separate clocks for each
of the T/H's, but because of their relationship to each
other, the clock signals can be generated from a simple,
end-around shift register. The "rotation" of the T/H's can
be accomplished by four six-input multiplexers, one for
each of the four multipliers. At each period, each multi-
plexer selects the appropriate T/H output for its
multiplier.
The overhead in implementing this architecture is small,
since the T/H's are now simply one-stage devices instead
of master/slave, and the extra hardware required consists of
several multiplexers and an easily generated set of clock
signals.

3. Circuit Descriptions

A chip was fabricated by MOSIS (MOS Implementation Services) in 2.0 μm CMOS with a four-
tap filter using the architecture of Figure 2. The T/H
clock registers utilized a high-speed single-phase D flip
flop design [9]. The control signals to the multiplexers
were obtained from the T/H clock signals through simple
combinatorial logic. The multiplexers were formed from
CMOS pass-gates and by themselves had a simulated band-
width of 54 MHz and a total harmonic distortion (THD) of .02% when driven by the buffer amplifier from
the T/H's. All THD figures are given for a .5 Vp-p 100
kHz sine wave. The T/H's and multipliers used are de-
scribed in Sections 3.1 and 3.2 respectively.

Figure 2  Circular FIR filter Architecture

3.1 Differential Track-and-Holds

The circuit in Figure 3 was used for the T/H's in the
design. A differential design and dummy switches were
used to reduce the magnitude of the hold step. The output
amplifier was a modification of the unity-gain amplifier in
[10].

Open loop T/H's in this 2 μm technology have
acquisition times of 4 to 10 ns and aperture times up to 4
ns [8]. These figures show that the T/H limits the
operation of a master/slave serial FIR filter to about 30
MHz. The hold settling time, or the amount of time
required for the held value to settle to within 1% of its
final value, was simulated to be 4.8 ns. By itself, the
hold settling time would limit the speed of operation of
our circular FIR filter to about 200 MHz. The output
amplifier had a simulated THD of 3.64% and a simulated
bandwidth of 82 MHz, when driven in "track" mode by the
input buffers to the chip.

3.2 Multiplying D/A Converters

An MDAC was chosen for this design instead of a fully
analog multiplier because the weights can be loaded into
the filter and it can be used with or without adaptation
(which would need to be implemented externally for this first-generation chip). Fully analog multipliers may be a better way to go, but they would require implementing either a fully adaptive filter or, at least, some form of weight updating scheme. For this first-generation design, neither of these approaches is justified.

Figure 3 Differential Track-and-Hold

A one-bit cell of the six-bit MDAC is shown in Figure 4. It consists of a differential voltage-to-current converter for the analog signal, and a set of digital switches that either steer the currents to the supply when that bit is off (=0), or to the output when that bit is on (=1). Thus transistors M1-M3 are always operating in saturation. This cell is used by itself for the least significant bit (LSB) and, in order to improve matching, is repeated twice for the next most significant bit, and then four times for the third bit. M3 is biased at 10 μA for all the cells used in the three least significant bits. For the three most significant bits, a compromise between matching and size is used. The basic cell is still that shown in Figure 4, but M3 is biased at 80 μA and copies of it are used to form the fifth and sixth bits. The linearity of the MDAC is inversely proportional to the W/L of transistors M1 and M2, which, along with the required signal bandwidth, dictated the transistor sizes.

A maximum differential non-linearity of 0.55 LSB's was measured in the fabricated MDAC's, and the measured THD varied from 1 to 2.1 % as the MDAC weights varied from zero to full scale, which was consistent with HSPICE simulations. Due to bandwidth limitations in other circuitry, the bandwidth of the MDAC could not be accurately measured, but was simulated at over 100 MHz.

4. Measurement Results

The chip consumed 148 mW at 30 Msamples/sec, and 95 mW at DC. The single-phase D flip flop clock shift register performed adequately at speeds up to 100 MHz.

For functional testing, we devised a test that would show the circular operation of the filter, as well as be able to isolate the outputs of individual T/Hs. Using an input that is high for one clock period and then low for the next five, the high signal will always be held by the same T/H. As this T/H "rotates" around the MDAC's, the output is equal to the input pulse multiplied by each weight in succession as shown in Figure 5. A slight modification of this test is to use a periodic input where the basic repeating unit is high for one clock cycle and low for six. In this way, each repetition of the pattern observed at the output is caused by a different T/H in the ring (and adjacent patterns are caused by adjacent T/H's). So by observing the pattern for six repetitions, we can see the matching between the T/H's and demonstrate the proper functioning of the MDAC's and multiplexers.

Figure 4 Multiplying D/A Converter Cell

Figure 5 Input and Output Waveforms

This waveform was generated by an arbitrary waveform generator and the output measured on an oscilloscope, triggered by the start of the input sequence. The results show that the circuit clearly functions properly up to 30 MHz, but the output degrades above that frequency and at 40 MHz the filter output was not correct. Figure 6 shows the measured input and output patterns at 1 MHz, and Figure 7 shows them at 30 MHz. Pattern noise is apparent in Figure 6 since the outputs of the different T/H's differ by as much as 1 LSB. The circuit was plagued by clock feedthrough at frequencies over 20 MHz.

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as is evident in Figure 7. The feedthrough is caused by inadequate isolation of analog and digital circuitry on the chip due to area constraints. The clock feedthrough is not a fatal problem since the disturbance that results is synchronous and does not affect the output when it is re-sampled by the detector, providing that the sample times are perfectly uniform. In practice, the feedthrough is undesirable since jitter on the sampling clock will be converted to voltage noise; but, it is difficult to quantify this effect.

Finally, Figure 8 presents the results of an idle channel noise measurement. The differential inputs were grounded, one weight was set to full scale and all of the others to zero, the chip was clocked at 30 MHz, and the output spectrum was measured. The white noise floor is $5 \times 10^{-14} \, \text{V}^2/\text{Hz}$, which corresponds to 850 $\mu$V rms in the 15 MHz Nyquist bandwidth. The clock feedthrough is observed at all multiples of 5 MHz since the T/H clock generation in eSSence involves a divided-by-six operation on the 30 MHz clock.

5. Conclusions

The circular FIR architecture has been implemented and proven to function as expected. The sampling rate of the filter was limited by the switching speed of the multiplexers, but this problem can be easily fixed and we expect the circuit to capable of performing at about 50 MHz in 2 $\mu$m CMOS.

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References


Figure 6 Functional test results at 1 MHz. The output (top trace) is about .3 V peak and the input (bottom trace) is about .5 V peak. The input pulses are 1 $\mu$s wide.

Figure 7 Functional test results at 30 MHz. The output (top trace) is about .3 V peak and the input (bottom trace) is about .5 V peak. The input pulses are 33 ns wide.
Figure 8  Idle channel noise spectrum, clock at 30 MHz