STG Decomposition and Its Correctness

Walter Vogler
Institute of Computer Science
University of Augsburg, Germany
vogler@informatik.uni-augsburg.de

Abstract

The behaviour of asynchronous control circuits can be specified with Signal Transition Graphs (STGs), i.e. Petri nets where transitions are labelled with rising and falling edges of circuit signals. Speed independent (SI) circuits (an important and robust subclass of asynchronous circuits) can be synthesized from STGs with tools like PETRIFY [3] and PUNF&MPSAT [6]. For this purpose, PETRIFY builds the reachability graph of the STG and, thus, suffers from state explosion; but also PUNF&MPSAT, which uses unfolding techniques of Petri nets, cannot deal with really large STGs.

An idea to overcome these limitations is to decompose the specification STG into component STGs by structural methods, such that these can be processed with a tool and the resulting circuits together implement the specification. This idea goes back to [2] and was worked out in a project together with Mark Schaefer, Dominic Wist, Ralf Wollowski, and Ben Kangsah; we also had the pleasure to cooperate with Victor Khomenko and Petr Jančar.

My talk will sketch the results of this project (see below for the relevant publications) with a special emphasis on the correctness notions we developed to prove that the STG components together indeed match the behaviour prescribed by the specification; cf. also e.g. [4, 5]. It should be mentioned STG decomposition methods have also been developed in [1, 16]. Both these approaches need a specification satisfying the so-called CSC-property, and checking this property for prospec-tive components is vital; here, [1] uses a behaviour approximation based on integer linear programming. In contrast, our method does not consider the behaviour of an STG, but is purely structural; this entails the promise that really large STGs can be dealt with.

References


∗This research was supported by the DFG-project ’STG-Dekomposition’ Vo615/8-2.


Asynchronous Network-On-Chip and its Potential

Tomohiro Yoneda
National Institute of Informatics
2-1-2 Hitotsubashi, Chiyoda-ku, Tokyo, Japan
yoneda@nii.ac.jp

Abstract

Recently, Network-on-Chip (NoC) architectures are considered to be a promising approach to implementing many-core systems, because in those systems, it’s not easy to design bus architectures which well scale with the system size. In this talk, we will focus on an asynchronous version of NoCs, where fully asynchronous on-chip networks are adopted. Compared to the corresponding synchronous design, an asynchronous NoC has several superior features; it needs neither clock skew handling (for a single clock system) nor resynchronization within each router (for a multi clock system), and has more tolerance against delay variations. We will discuss how to design, implement, and apply an asynchronous NoC to make the best use of its potential.