Performamnce evaluation of five stage VCO ring oscillator with reverse substrate bias and SAL technique using nanoscale CMOS technology

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***Abstract*—In the present work, improved designs for five-stage voltage controlled ring oscillators (VCO) with reverse body bias and SAL technique have been presented to improve the performance parameter. First VCO design with inverter based delay cell shows frequency variation [3.9-1.89] MHz with SAL technique and Second design with varying PMOS and NMOS substrate bias from [0.6-1.1] V shows frequency variation of [6.62-3.0] GHz. The proposed five stages VCO ring oscillator is implemented in 45nm cadence virtuoso environment provides high oscillation frequency (GHz) provide less delay (0.21psec), minimum phase noise (179.1dBc/Hz) and lower leakage power (1.23pw) with reverse substrate bias technique.**

Keywords-VCO Ring oscillator; SAL; Delay; Leakage Power ; Oscillation frequncy; Phase noise.

I. INTRODUCTION

The main challenge in nanoelectronic is to develop information-processing system based on nanodevices, information storing circuit and frequency signal generating circuit mainly supported by information-processing circuit [1][2]. The voltage controlled oscillator (VCO) is the core factor of Phase locked loop (PLL) oscillation frequency synthesizes, which is mainly used in modern electronics information processing systems [4]. Oscillatory behavior is ubiquitous in all physical systems, especially in electronic and optical. In radio frequency and light wave communication systems, oscillators are used for frequency translation of information signals and channel selection [9][17]. Oscillators are also present in all digital electronic systems, which need a time reference, i.e., a clock signal, in order to synchronies operations. An ideal oscillator would provide a perfect time reference, i.e., a periodic signal [3]. However, all physical oscillators are corrupted by undesired perturbation/noise. Hence signals generated by practical oscillators are not perfectly periodic, since oscillator is a noisy physical system and it makes them unique in their response to perturbation/noise [12]. A variety of oscillators is available but the principle of operation; the frequency band of oscillation and the performance in noisy environment are different from one class of oscillators to the other [21]. Recently, communication transceiver design in single IC has demanded monolithic oscillator with low-cost and low power dissipation [6]. In this system, the design of ring oscillator using delay stages inside the IC has created much more importance compared to other monolithic oscillators like relaxation oscillators [7]. Generally, the performance of ring oscillator is better than relaxation oscillators, although not as good as that of the sinusoidal oscillators [8]. However, the continuous efforts of the scientists and researchers have yielded in improving the performance of ring oscillators to attain a good level of satisfaction, which can now be used successfully in the communication systems. The level of satisfaction has been achieved in both cases: speed of operation and noise performance. The main object of the paper is to enhance the performance (phase noise, delay, leakage power, oscillation frequency) of VCO ring using SAL and reverse substrate bias technique and provide a comparison between them.

II. CIRCUIT DESCRIPTION

A. VCO ring oscillator

Ring oscillator is cascaded combination of delay stages, connected in a close loop chain [8] [9].

The ring oscillators designed with a chain of delay stages have created great interest because of their numerous useful features. These attractive features are: (i) It can be easily designed with the state-of-art integrated circuit technology (CMOS, BiCMOS), (ii) It can achieve its oscillations at low voltage, (iii) It can provide high-frequency oscillations with dissipating low power, (iv) It can be electrically tuned, (v) It can provide wide tuning range and (vi) It can provide multiphase outputs because of their basic structure [23].

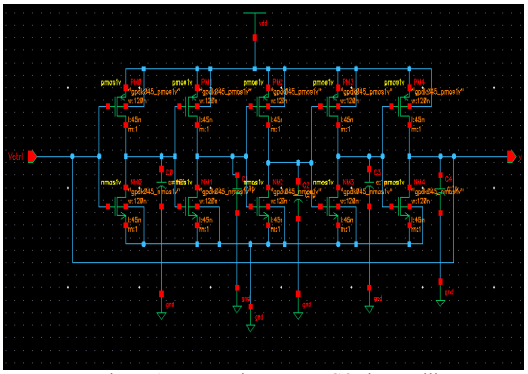

Figure 1 Five stage VCO ring oscillator

Figure 1 shows the five stages VCO ring oscillator using an inverter combination with capacitor 0. 01pf.

These outputs can be logically combined to realize multiphase clock signals, which have considerable use in a number of applications in communication systems [9]. The

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oscillation frequency of an RO depends on the propagation delay per stage, and the number of stages used in the ring structure [11].

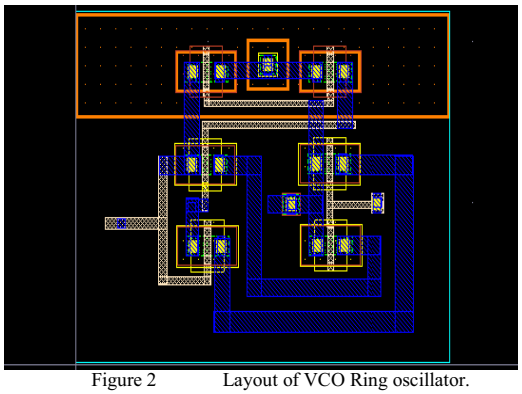

Figure 2 Layout of VCO Ring oscillator.

Figure 2 shows the layout of five-stage VCO ring oscillator

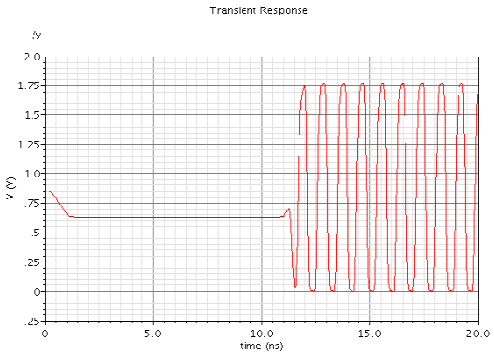

Figure 3 Waveform of VCO Ring oscillator.

Figure 3 shows the five-stage VCO ring oscillator at rise and fall time is 1ns and pulse width is 20ns.

B. Sub circuit of VCO ring oscillator (inverter)

Five stages VCO ring oscillator consists of five inverter configuration. Inverter is designed by using one NMOS and one PMOS transistor. PMOS transistor works as pull-up network and NMOS transistor works as a pull-down network. In this combination, PMOS transistor is connected to power supply and NMOS transistor is connected to be ground. Inverter schematic and its working region given as

$$I_D = 0(\text{off: } |V_{GS}| < |V_{TH}|) \quad (1)$$

$$I_D = k * \left(\frac{W}{L}\right)\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right](\text{triode: } |V_{DS}| \leq |V_{GS}| - V_{TH}) \quad (2)$$

$$I_D = \left(\frac{k}{2}\right) * \left(\frac{W}{L}\right) * (V_{GS} - V_{TH})^2 * (1 + \lambda n, pVDS \text{saturation: } VDS \geq VGS - VTH \quad (3)$$

We have following regional relation

$$\text{NMOS}\begin{cases} V_{out} > V_{DD} - V_{Tn}: \text{off} \\ V_{in} \leq V_{DD} - V_{Tn}: \text{triode} \\ V_{in} \geq V_{DD} - V_{Tn}: \text{saturation} \end{cases} \quad (4)$$

$$\text{PMOS}\begin{cases} V_{in} < -V_{Tp}: \text{off} \\ V_{out} \geq -V_{Tp}: \text{triode} \\ V_{out} \leq -V_{Tp}: \text{saturation} \end{cases} \quad (5)$$

In above equation V_{GS}= gate to source voltage, V_{DS}= drain to source voltage, V_{TH}= threshold voltage

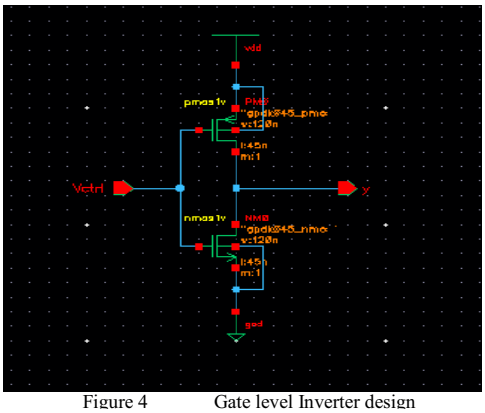

Figure 4 Gate level Inverter design

Figure 4 shows the inverter schematic diagram using PMOS and NMOS where Vin (06v to1.1v)

C. VCO ring oscillator with SAL technique

1) Self-adjustable voltage level circuit (SAL)

Fig. 3 shows the general self-adjustable voltage level circuit [25], where Vdd is the supply Voltage, and VL is the output voltage of this circuit, which is applied to any load circuit during the active mode (when SL=0). This circuit supplies greatest supply voltage to the load circuit through the ON PMOS transistor (P1) so that the load circuit can operate quickly. During the standby mode (SL=1), it provides slightly lower supply voltage to the load circuit through the weakly ON NMOS transistors (N1, N2, N3 --- Nm). So the voltage applied to the load circuit is given by.

$$V_L = V_{DD} - V_N \quad (6)$$

Where Vn is the voltage drop of m weakly ON NMOS transistors and drain to source voltage Vdsn of the OFF NMOS in the standby mode is expressed as.

$$V_{dsn} = V_L - V_{SS} = V_L \quad (7)$$

Vdsn can be decreased by increasing Vn that is rising m, the number of NMOS transistors. When Vdsn is decreased, the drain- induced–barrier-lowering (DIBL) effect is decreased and this in turn increases the threshold voltage Vtn of NMOS transistors. so, the sub threshold leakage current of the OFF MOSFET decreases, so leakage power is minimized, while data are Retained [6]. Fig. 3 shows the proposed leakage power reduced five-stage VCO ring oscillator design using self-adjustable voltage level circuit.

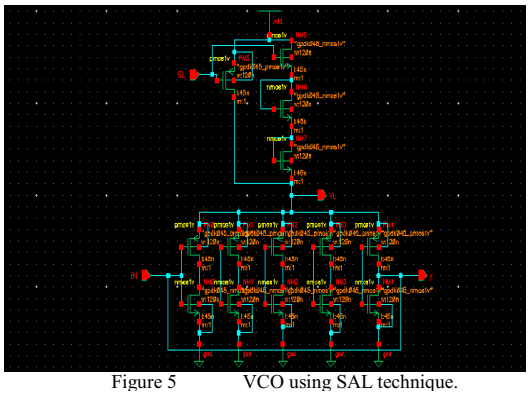

Figure 5 VCO using SAL technique.

Figure 5 shows the five stages VCO ring oscillator with SAL technique in which power is reduced up to6.49µw at 0.6v input supply.

D. Five stage vco ring oscillator with reverse substrate bias technique

Bulk terminal of PMOS and NMOS have been used for controlling the output frequency and reduction in power consumption in VCO structure. By application of reverse body bias, the Vth is increased as given in equation (8), which subsequently reduces the sub threshold leakage currents [5], Bulk terminal of PMOS and NMOS have been used for controlling the output frequency and reduction in power consumption in VCO structure. By application of reverse body bias, the Vth is increased as given in equation (1), which subsequently reduces the sub threshold leakage currents [5][26]. Threshold voltage (Vth) is related by the square root of the bias voltage implying that a considerable voltage level would be needed to raise the Vth. By controlling bulk voltage (Vsb) leakage current are minimized and hence power consumption is reduced.

$$V_t = V_{to} + \gamma\left(\sqrt{2\emptyset_f} + V_{sb} - \sqrt{2\emptyset_f}\right) \quad (8)$$

Where Vto is threshold voltage for Vsb = 0V; $\emptyset_f$ is Fermi potential and γ is substrate bias co efficient.

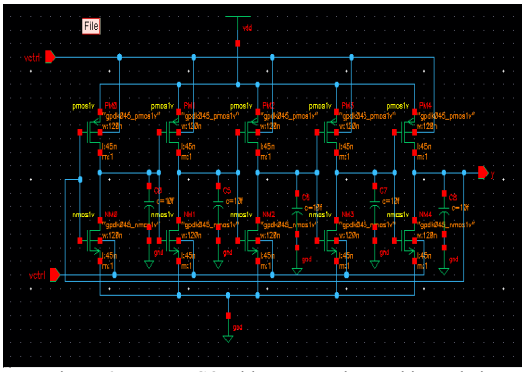

Figure 6 VCO with reverse substrate bias technique.

CMOS inverter has been utilized as the delay element in the proposed circuits. Each inverter stage is made up of NMOS and PMOS pair and body terminal of transistors are not connected to source [23]. A small capacitance of 0.01pf at output of each delay cell has been included. The circuits have been designed in 45nm CMOS technology with supply voltage of 0.7V. In this configuration circuit NMOS substrate bias (Vn) and PMOS substrate bias (Vp) have been varied simultaneously as shown in Fig. 5. All PMOS and NMOS transistor substrate terminal have been biased to (Vp andV_n) which have been varied from 0.6 to 1.1V. Supply voltage also has been fixing at 0.7v. Output frequency have been controlled by combination of NMOS, PMOS reverse biasing and supply voltage.

Figure 6 shows the five-stage VCO ring oscillator with reverse substrate bias technique and reduced power 1.23pw and delay are 0.21psec at 0.6v input supply.

III. SIMULATION RESULT

The circuit works simulated in cadence for 45nm technology, from the result table, we can observe reverse substrate bias technique provide effective percentage reduction in delay and power as compared to SAL technique.

A. Leakage power

Leakage power is an important factor for any CMOS design circuit. The leakage current is directly related to the electric field of the device. By reducing the node voltages decrease the leakage current [6]. In other words, we can say that leakage power is a waste charge of any device, which is regularly discharging from the device even the device in off state. It reduces the capability of the device also became the reason of poor performance of the device.

In the VCO power consumption is given by as

$$\text{Power consumption} = C_l * V_{dd} * f \quad (9)$$

WhereC_L is load capacitance, Vdd is power supply in VCO (0.7V in 45nm technology), f is frequency of VCO [16].

TABLE I. LEAKAGE POWER ANALYSIS IN 45nm TECHNOLOGY

Voltage	Leakage power in SAL	Leakage power in Reverse substrate bias
0.6V	6.49µW	1.23pW
0.9V	8.84µW	1.88nW
1V	20.53µW	2.94nW
1.1V	28.22µW	3.59nW

Table I shows the leakage analysis in five stages VCO ring oscillator with SAL and reverses substrate bias technique and provide a better simulation results in reverse substrate bias technique (1.23pw).

In the five stages VCO ring oscillator minimum leakage power is given by reverse substrate bias technique at 0.6V.

Leakage Power with SAL technique (input voltage 0.6v) = 8.84µw (10)

Leakage power with reverse substrate bias technique (input voltage 0.6v) =1.23pw (11)

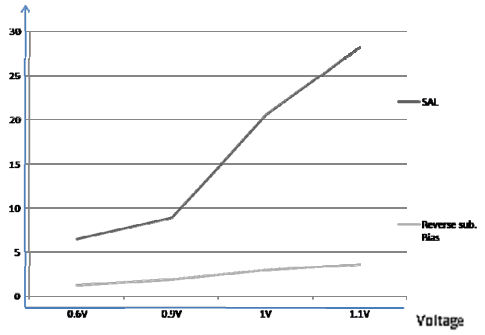

Figure 7 Power analysis of VCO ring.

Figure 7 shows the leakage power analysis of five-stage VCO ring oscillator with reverse substrate bias and SAL (self-adjustable adjustable level) technique at different voltage.

B. Oscillation frequency

The VCO is a useful analog circuit main reason of that its oscillation frequency (F_{osc}) can be set to a desired value [10] [16].

The Governing equation for a VCO is given by as

$$F_{osc} = F_o + K_{vco}V_{ctrl} \quad (13)$$

In above equation F_o is center frequency of VCO, K_{vco} is gain of the VCO, V_{ctrl} is input of VCO

Frequency of oscillation for N stage Delay VCO is given by following equation as

$$F_{osc} = \frac{1}{2NT_d} \quad (14)$$

Where N is the Number of delay stages and t_d is delay of each stage [23].

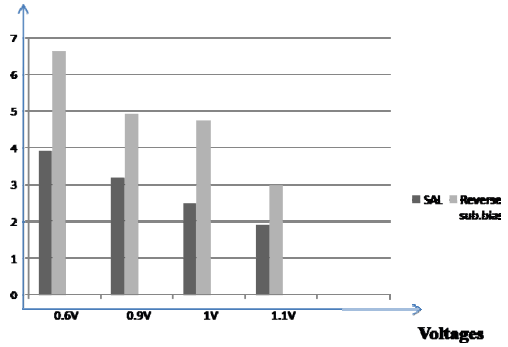

Figure 8 Oscillation frequency of VCO ring oscillator

Figure 8 shows the comparative study of reverse substrate bias and SAL technique in five-stage VCO ring oscillator in 45nm technology.

Max oscillation frequency of five stage VCO ring oscillator with reverse substrate bias technique in 45nm technology at 0.6V, where N=5, delay t_d= 0.21psec so the oscillation frequency F_{osc}=6.62GHz

TABLE II. OSCILLATION FREQUENCY ANALYSIS

Voltage	Oscillation frequency in SAL	Oscillation frequency in Reverse substrate bias
0.6V	3.9Mhz	6.62Ghz
0.9V	3.2Mhz	4.92Ghz
1V	2.5Mhz	4.73Ghz
1.1V	1.89Mhz	3.0Ghz

Table II shows the oscillation frequency of five-stage VCO ring oscillator. Reverse substrate bias technique provides 6.62GHz oscillation frequency at 0. 6v input supply comparatively better than SAL technique (3.9MHz).

C. Delay

The time difference between the input increasing the reference voltage and output changing the logic state is known as the propagation delay.

The common gate delay time of a ring oscillator td is calculated from its oscillation frequency f0 by [23]

$$t_d = \frac{1}{2.n.f_0} \quad (15)$$

In the five-stage ring oscillator, delay is reduced with reverse substrate bias technique voltage ranges from (0.6 to 1.1v) in 45 nm technology; minimum delay is 0.21psec at 0. 6v.

TABLE III. DELAY ANALYSIS I

Voltage	Delay in SAL	Delay in Reverse substrate bias
0.6V	25.2nsec.	0.21psec.
0.9V	30.6nsec.	1.51psec.
1V	39.4nsec.	2.016psec.
1.1V	52.9nsec.	3.33psec.

Table III shows the delay analysis of five-stage VCO ring oscillator reverse substrate bias technique provides less delay (0.21psec).

D. Phase noise

Phase noise is the frequency domain representation of quick, short-term, random fluctuations in the phase of a waveform, caused by time domain instabilities [4][12].Phase noise is added to this signal by adding a stochastic process represented by φ to the signal as follows:

$$v(t) = A\cos\left(2\pi f_0 t + \varphi(t)\right) \quad (16)$$

Phase noise is a type of cyclostationary noise and is closely related to jittering [13]. A particularly important type of phase noise is that produced by oscillators.

Phase noise is classically expressed in units of dBc/Hz, and it represents the noise power relative to the carrier contained in a 1Hz bandwidth centered at a certain offset from the carrier [22].

In the five-stage ring oscillator phase noise measure in 45 nm technology with SAL and reverse substrate bias technique (i.e.123.4dBc/MHz and 179.1dBc/ μ Hz) respectively.

TABLE IV. PHASE NOISE ANALYSIS.

Voltage	Phase noise in SAL	Phase noise in Reverse substrate bias
0.6V	123.4dBc/mHz	179.1dBc/µHz
0.9V	139.1dBc/mHz	180.6dBc/µHz
1V	144.0dBc/mHz	182.3dBc/µHz
1.1V	148.7dBc/mhz	185.2dBc/µHz

Table IV shows the phase noise analysis of five-stage VCO ring oscillator with reverse substrate bias and SAL technique. SAL technique provides more phase noise (123.4dBc/mHz) at 0.6v input supply.

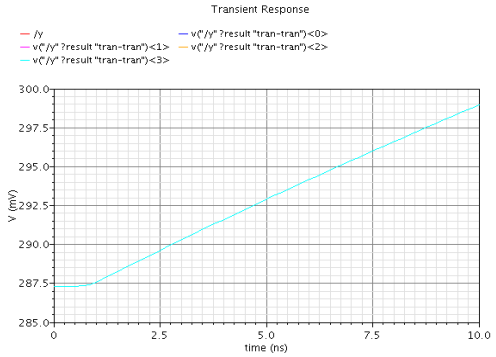

Figure 9 Phase noise of VCO ring oscillator

IV. CONCLUSION

In reported work, two techniques are used to improved designs for five-stage CMOS inverter based VCO have been presented. By controlling of reverse body bias power consumption has been low, and output frequency has been controlled with the advantage of full swing output signal. Controlling the bulk terminal provide an alternative method to control the output frequency with reduced power consumption (1.23pw). For first proposed VCO frequency range of [3.9 to1.89] MHz with SAL technique and leakage power is 8.84µw at 0.6v input voltage. Output frequency range [6.62 to 3.0] GHz has been obtained with joint biasing of NMOS & PMOS transistors with Vdd = 0.7v in 45nm technology. Manoj Kumar [27] used reverse substrate bias technique, which provide 0.467mW leakage power and 1.3GHz at Vdd=1.8v in 0.18µm technology. Simulations provide better results in reverse substrate bias in comparison to SAL (self-adjustable adjustable level) technique. Power saving can be achieved by applying reverse biasing with constant supply voltage for those applications in which limited frequency variation is desired.

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