Design of High Speed and leakage Tolerant CMOS Comparator in UDSM Technology

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***Abstract*— In modern digital VLSI design, domino logic style circuits are widely used. The CMOS domino logic circuit dissipates very low standby power and exhibits less area. We design a comparator circuit which uses footed domino logic and also implement a current mirror circuit in the design, to enhance the speed of the comparator. This paper emphasizes a CMOS comparator design to detect full match or mismatch of the binary input. The proposed design consumes low leakage power and had a higher speed, than other circuit. The delay, leakage power and average power of the proposed CMOS Comparator circuit have also been calculated and then it is compared with the Footed Domino Logic Comparator circuit with same parameter. The circuit has been simulated in 45nm CMOS technology on Cadence Tool for high fan-ins (4, 8, 16, 32& 64 bits).**

Keywords- Domino logic; leakage power; delay; comparator; UDSM

I. INTRODUCTION

Comparator are the most important design element for various application such as in embedded processor, general purpose processor, DSP core, image/signal processing and built in self test circuits [1].Minimizing the power dissipation for the digital circuits requires optimization at all level of the design. So, this optimization depends on circuit style, topologies and in fact includes the technology which is used to implement the digital circuits [2]. Dynamic Domino style circuits offers good performance and wide fan-in logic as compared to static CMOS logic [3]. This Domino CMOS logic is capable for high performance circuits because it offers higher speed than static CMOS circuits. This paper deals with CMOS comparator in UDSM range, using Footed Domino Logic Style Comparator(FDLC) in the circuit, which is use to detect full match or mismatch of the binary input applied to the circuit [4]. To achieve low leakage and higher speed, a current mirror circuit is added in the FDLC circuit. The leakage power, average power and delay of the proposed CMOS comparator circuit is calculated for 4, 8, 16, 32 and 64 bits. The simulation results are obtained at 45nm CMOS technology using Cadence Virtuoso Tool. This paper organized in such a way that, after the introduction part in section I, section II explains the previous work, section III describes the power and delay expression of the circuit, section IV gives brief description of proposed comparator circuit, section V includes simulation and result and finally section VI manipulates summary and conclusion.

II. PREVIOUS WORK

The schematic of Footed Domino Logic Comparator shown in figure 1. The N-foot transistor reduces the total power consumption and also improves the noise immunity [5]. The FDLC circuit is used in modern data path, where the mismatch occurs with a much higher frequency as compared to full matches. So, it will be inefficient that the circuit dissipate energy only on a full match and almost no energy on mismatch [5] [6].

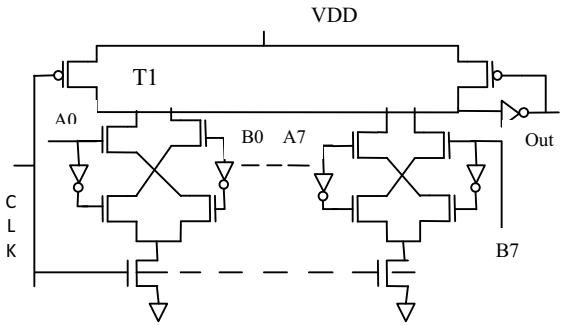

Figure 1. Footed Domino Logic Comparator

The footed domino logic comparator circuit's exhibit low leakage power, but on the other hand FDLC circuit has lower speed than footless domino logic comparator circuit and also an overhead. This comparator circuit simulated in 70nm CMOS predictive models. The power supply applied in this circuit was 0.9v, due to which dissipate low power but it has low speed, which is overcome in the proposed comparator [5].

III. POWER AND DELAY EXPRESSION

The average power consumption of the circuit requires some input vectors to obtain accurate estimation [7]. The average power over the interval is [8]

$$\text{Pavg} = \frac{E}{T} = \frac{1}{T}\int_0^T i_{DD}(t)\, V_{DD}\,\text{dt} \qquad (1)$$

Where E is the energy consumed over some time interval T is the integral of instantaneous power.

$$\text{E} = \int_0^T i_{DD}(t) V_{DD}\, dt \qquad (2)$$

P (t) is the instantaneous power drawn from power supply is proportional to supply current i(t) is supply voltage VDD.

$$P(t) = i(t)V_{DD} \qquad (3)$$

In CMOS inverter circuit, three types of power dissipation occur.

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A. Leakage power dissipation

When static current flows from VDD to ground node without degrading inputs are called leakage power [9]. The main components of leakage power in the OFF state at band to band tunneling, sub-threshold leakage (I sub), gate induced drain leakage, gate tunneling leakage.

B. Short circuit power

From α-power law [10], the short circuit power dissipation model is

$$P_{sht.ckt.power} = V_{DD} t_T I_{Do} \frac{1}{\alpha+1} \frac{1}{2^{\alpha-1}} \frac{(1-2v\ )^{n+1}}{(1-v_T)^{\alpha}} \quad (4)$$

$$\text{Where } V_T = \frac{V_{TH}}{V_{DD}}$$

C. Dynamic power dissipation

Dynamic power dissipation is associated with switching of transistor from high to low and low to high, i.e. due to the charging and discharging of load capacitance [9] [11].

$$D_{ynamic} = \alpha C_L {V_{DD}}^2 f \quad (5)$$

Where, α is switching activity factor of gate.
C_L is load capacitance.
V_{DD} is supply voltage.
F is operating clock frequency.

In CMOS digital circuits, the gate delay time (t_{pd}) is given by equation 6. [12]

$$T_{pd} \alpha \frac{CV_{CC}}{(V_{CC}-V_t)^{\alpha}} \quad (6)$$

Where,

Tpd is gate delay
V_t id threshold voltage
α is activity factor
V_{cc} is supply voltage

IV. PROPOSED COMPARATOR

Our proposed Comparator circuit is implemented in 45nm CMOS technology, with a supply voltage of 0.7V due to which the circuit exhibits low leakage, less average power dissipation, than other works. The schematic of high speed and a leakage tolerant CMOS comparator based on Footed Domino Logic comparator shown in figure 2.This proposed comparator indicates the full match or mismatch of the two binary inputs A and B of 4, 8, 16, 32 or 64 bits applied to the circuit. Basically, this circuit operates on two modes, one is precharge mode and another is evaluation mode. In precharge phase, the clock is low, which makes transistor T1 ON and T2 OFF, then the precharge node is precharge to high and the output goes low and T2 turns ON. This PMOS transistor T2 keep providing the supply to the pull down network, hence it is known as Keeper Transistor, and Transistor T1 is known as Precharge transistor. During the evaluation mode, when the clock is high, if the corresponding bits of A and B inputs are same than there is no conduction path from precharge node to ground, hence the output remains low. But, if any position of input A and B are differ than there will exists a conduction path from precharge node to ground, which causes the discharging of that node and hence the output goes high. So, when the output become high, then the keeper transistor T2 turns OFF, this makes the output high [5] .To provide sacking effect for leakage reduction in evaluation phase transistor T7 is added, but due to this there is an increase in delay, so for reducing the delay in evaluation phase, a current mirror (T8) is added in parallel with evaluation network. The T9 transistor is used to provide feedback from the output to dynamic node, to avoid short circuit current on static inverter [13]. This additional circuit in proposed comparator work in such a way that, in precharge phase, the precharge node is high, then the footer transistor T6 is OFF, therefore the current mirror (T8) is also OFF, and then there is no path for the discharging of precharge node. In case of evaluation phase, if all inputs are same then stacking effect offered by transistor T7 reduces the leakage of evaluation network [13] [14]. However, when the one of input bit is differ, T8 mirror transistor pulls large current from precharge node, since the output goes to high T9 transistor gets ON to discharge the precharge node completely. So T7 and T8 transistor makes the circuit faster in evaluation phase [5][13][15].

V. SIMULATION AND RESULT

Simulation is performed in Cadence tool using analog design environment (ADE) in 45nnm process technology to enable a fair comparison with previously reported comparator, which was implemented in 70nm process technology. The delay, leakage power, and average power is calculated for high fan in 4, 8, 16, 32 & 64 bits of the Footed Domino Logic Comparator circuit and proposed comparator circuit. These parameters are calculated with the supply voltage of 0.7V, Period = 2.5ns, Pulse width = 1.25ns, initial delay= 0 nS. The result for the comparison of FDLC circuit and proposed comparator circuit for low power and high speed is listed in Table 1. Figure 3 and figure 4 indicate the transient response of the proposed comparator circuit, which relates the input and output waveform w.r.t to time in ns. From figure 3, it can be observed that the output remains low for precharge and evaluation phase, since all the corresponding input bit of A and B are same, so there is no conduction path for the discharging of precharge node. Hence the output remains low for the evaluation mode [16]. From figure 4, it can be evaluated that output is low for the precharge phase but it goes high in evaluation phase, since one of the corresponding input bit or may be more than one input bit of A and B is different, which produces conduction path to discharge the precharge node. Hence the output goes high for evaluation phase. Table 1 shows the comparison between FDLC and proposed comparator circuit in terms of leakage power, average power and delay. This table indicates that the leakage power, average power and the delay of the proposed comparator reduced with respect to the FDLC circuit.

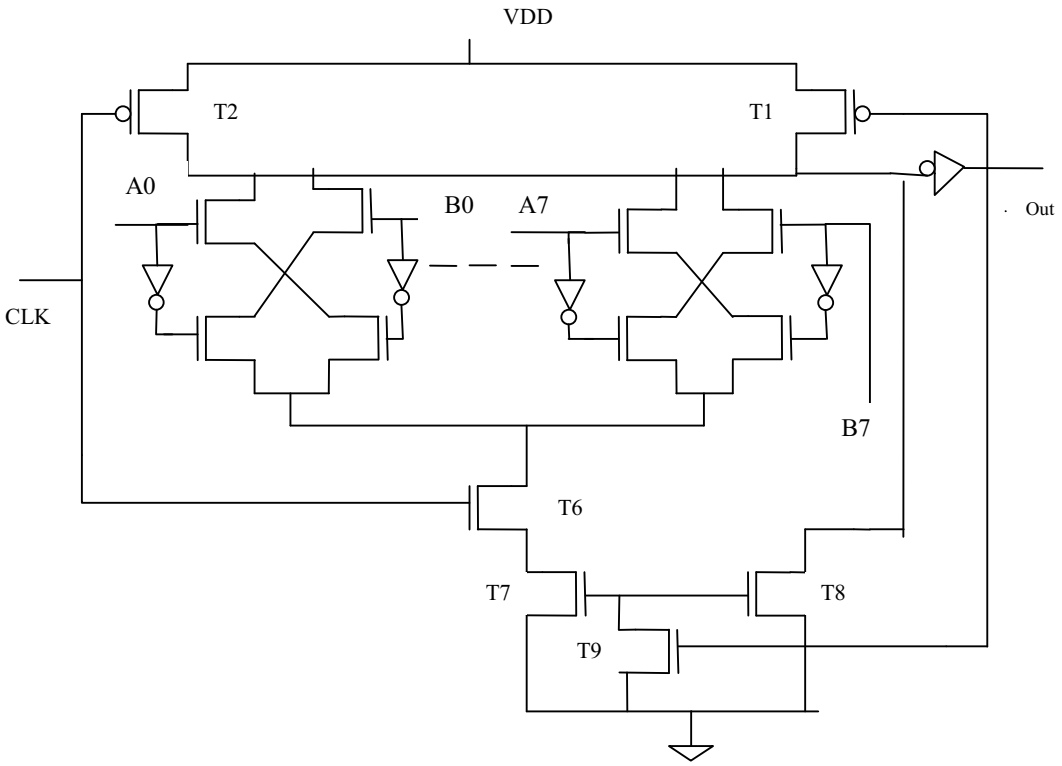

Figure 2. Proposed Comparator

TABLE I. SIMULATION RESULTS OF FDLC CIRCUIT AND PROPOSED COMPARATOR CIRCUIT

Bits	FDLC Circuit			Proposed Comparator		
	Leakage Power (nW)	Average Power (mW)	Delay (ns)	Leakage Power (pW)	Average Power (mW)	Delay (pS)
4	11.14	278.39	482.65	5.103	282.52	231.97
8	22.68	289.34	598.74	14.71	277.01	416.50
16	44.59	245.49	674.33	23.81	268.30	502.60
32	66.26	263.88	751.96	32.05	263.40	582.12
64	95.70	255.97	821.10	49.91	249.87	649.23

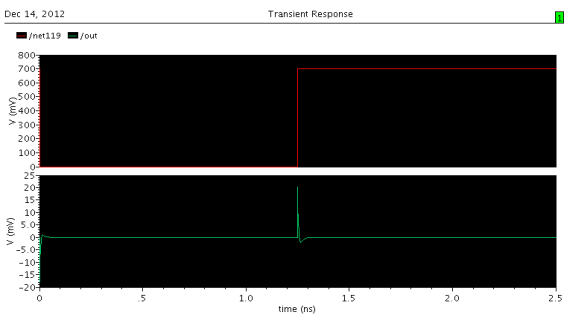

Figure 3. Transient response of proposed comparator, when input bits of A and B are same.

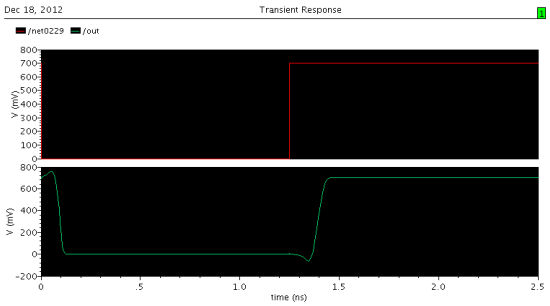

Figure 4. Transient response of proposed comparator, when input bits of A and B are different

VI. CONCLUSION & SUMMARY

Power and speed being a limiting factor for high performance and high density integrated chips, without affecting the performance of the circuit, a great effort has been put to explore low leakage power and high speed [17]. Domino CMOS logic dissipates very low standby power compare to static CMOS logic [18], in our proposed circuit we use footed domino logic comparator circuit .We proposed a comparator circuit which is suitable for UDSM CMOS technologies. This paper gives the comparison of footed domino logic comparator circuit and proposed comparator in terms of leakage power and delays for high fan in 4, 8, 16, 32 & 64 bits. It has been found from the simulation result that the leakage power and delay of the proposed comparator reduces as compare to Footed Domino Logic Comparator circuit. These comparisons of the comparator design are based upon 45nm CMOS technology in Cadence tool.

VII. ACKNOWLEDGEMENT

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