Design of an Ultra Wideband Low Noise Amplifier(LNA) Circuit with High Center Frequency and Low Power Consumption

Md. Asif Mahmood Chowdhury
Department of Electrical & Electronic Engineering
Bangladesh University of Engineering & Technology
Dhaka, Bangladesh.
Email: asifmahmood200606107@gmail.com

Prasenjit Chowdhury
Department of Electrical & Electronic Engineering
Khulna University of Engineering & Technology
Khulna, Bangladesh.
Email: pcjony09@yahoo.com@gmail.com

***Abstract*—A LNA (Low Noise Amplifier) circuit with high centre frequency and ultra wide bandwidth is designed. IBM 90nm CMOS process is used to design this circuit. Centre frequency of this LNA circuit is 18.3 GHz. At the centre frequency gain is 14.38 decibel. 5.7 GHz is the -3 dB bandwidth of this LNA circuit. It can be operated from around 14.2GHz to around 19.9 GHz with considerably high gain. Performance of this LNA circuit is verified by simulation. This circuit has a power consumption of this circuit is 64.63 micro-watt. Required supply voltage for this LNA circuit is 1.4V.**

Keywords- High centre frequency; Ultra-wideband ; low power consumption ; low supply voltage ; high gain ; cascade stage .

I. INTRODUCTION

Ultra-Wideband (UWB) is a wireless technology which can work with very low power for a short distance communication. High centre frequency, wide bandwidth are important features of ultra wideband technology. Low cost implementation of the UWB promises high throughput at short distances without interfering with other existing wireless communication system [1].

In our design, we have proposed a Low Noise Amplifier (LNA) for a UWB receiver using IBM 90nm CMOS process. LNA is the first block of the UWB receiver end. It amplifies the transmitted signal received by the receiving antenna. We have used CS-CS (Common Source-Common Source) Cascode stage topology of LNA, as this topology offers higher gain and bandwidth compared to other topologies of LNA implementation [2]. We have included differential output in our design as it gives better immunity against noise due to supply voltage variation [3].

After system level analysis, the proposed circuit has been simulated in circuit level. In the simulation stage, we have focused on optimizing LNA parameters like gain, bandwidth, center frequency, power consumption etc. From circuit level simulation, the gain is found to be around 14.32dB with center frequency of 18.3GHz. The bandwidth is around 5.7 GHz which is about 28% of the centre frequency. This is a promising finding since UWB process requires the bandwidth to be at least 20% of the centre frequency. Besides the power consumption of our circuit is around 64.63 microwatts which is also a optimistic result in terms of power dissipation.

In a word, despite being a circuit level simulated design, our design promises to bring out a highly effective LNA system through the process of further development.

II. SCHEMATIC DESIGN

Schematic design for our LNA circuit is given below :

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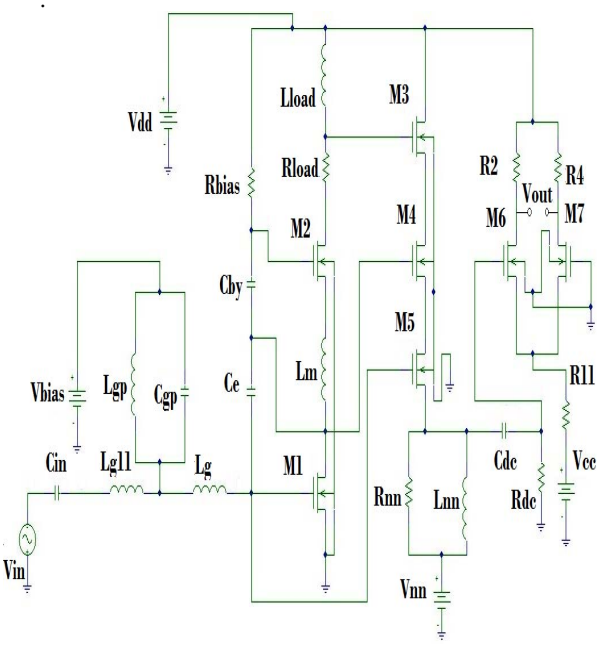

Fig. 1 Schematic of LNA

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DOI 10.1109/ACCT.2013.74

Our design is a modified version of a previously proposed LNA circuit [4]. There was a current source which is replaced by a current mirror circuit. This current mirror circuit exists between source of MOSFET (M5) and ground. A high pass filter circuit is placed between source of MOSFET (M5) and gate of MOSFET (M6). This high pass filter circuit is due to the elimination of DC offset voltage in the output waveform. At the end, our output of the circuit is differential output. We get this differential output from node between drain of MOSFET(M6) & resistor (R2) and node between drain of MOSFET(M7) & resistor (R4) as shown in figure.

III. Time Domain Analysis

At first we have done transient analysis of our LNA circuit. Here, transient response of this LNA circuit is shown below. At this case, frequency of input signal is 18 GHz.

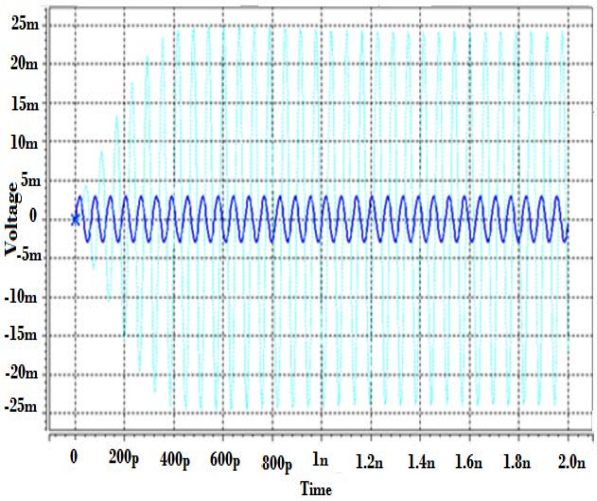

Fig. 2 Wave form of input (dark blue) and output signal (light blue)

In the above graph , voltage is shown along Y axis whose unit is volt and time is shown along X-axis whose unit is second. In case of voltage , we found our wave form in milivolt level and in case of time wave form is in pico and nano second level . Here, wave form of input and output signal are shown simultaneously . Here, amplitude of input signal is 6 mV peak to peak . Amplitude of output signal is 50 mV peak to peak. This time domain response is for the input signal's frequency of 18 GHz. From the above graph we observed that at first output signal was in transient condition . After a transient period of 400 pico-second the output signal has reached to steady-state condition. At steady-state period, output wave shape is purely sinusoidal like the shape of input signal.

IV. Frequency Domain Analysis

After time domain analysis frequency domain analysis has been performed. In this analysis we have calculated gain at centre frequency . Next -3 dB bandwidth has been calculated. For being ultra wide band this -3 dB bandwidth should be at least 20% of center frequency. Wave form of frequency domain analysis is given below.

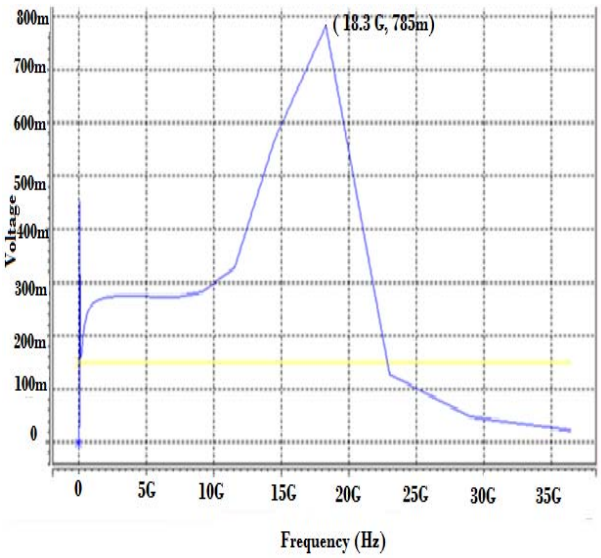

Fig. 3 Frequency response of output signal(deep blue) and input signal (yellow) (peak amplitude voltages are shown)

In the above figure, along Y-axis voltage is shown and unit is volt. Frequency in hertz is shown along X-axis. Here, peak amplitude voltages are shown and these wave forms are in milivolt level. In case of frequency these graphs are in giga hertz level.

Input signal's change with respect to frequency is shown by yellow straight line. This is a straight line because we have given input signals of same amplitude which is 150 milivolt (peak amplitude voltage) but of different frequencies to observe the effect of frequency on output voltage amplitude .

In case of output signals, from the range of frequency starting to 10 GHz , peak amplitude of the input signal is almost constant. From frequency 10 GHz there is a sharp increase in the peak amplitude of output signal till 18.3 GHz. Peak amplitude of output signal reaches to it's highest value at 18.3 GHz and it is 785 milivolt (peak amplitude voltage) . So , centre frequency of this circuit is 18.3 GHz . After this frequency, peak amplitude of output voltage begins to fall . We have observed a sharp fall from 18.4 GHz to around 23 GHz . After 23 GHz the peak amplitude of output signal continues to fall but graph is less steeper.

It can be inferred that this circuit can be operated from around 14.2 GHz to around 19.9 GHz with considerably high gain .

A. Gain Calculation :

We will calculate gain at center frequency in decibel (dB).
From graph,
We get, peak amplitude of input signal is 150 milivolt and peak amplitude of output signal is 785 milivolt. (At centre frequency)
Gain at centre frequency = $20 * \log_{10}(Vout(p) / Vin(p))$ dB

$= 20 * \log_{10}(785m / 150\ m)$ dB

$= 20 * \log_{10}(5.233)$ dB

= 14.38 dB.

This is the highest voltage gain of our proposed circuit which is occurred at centre frequency . Above or below of this centre frequency the voltage gain of the circuit will be less.

B. Band-width Calculation :

Bandwidth of any circuit will give us idea about the range of frequency in which the circuit can be operated with considerable high gain .
For finding -3dB bandwidth we have to find corresponding output voltage due to gain of (14.38-3) or 11.38 dB. We know that ,

Gain in decibel = $20 * \log_{10}(Vout\ (p)/ Vin\ (p))$ dB.

Here , gain is 11.38 decibel and Vin (p) is 150 milivolt . From the above equation we get

Vout(p) =Vin (p) * antilog (Gain in decibel/20) milivolt

= 150 * antilog (11.38/20) milivolt

= 150 * 3.7068 milivolt

= 556.021 milivolt

Now, we have to find two frequencies for which output peak amplitude will be 556.021 milivolt. Difference between these two frequencies is defined as -3 dB bandwidth.

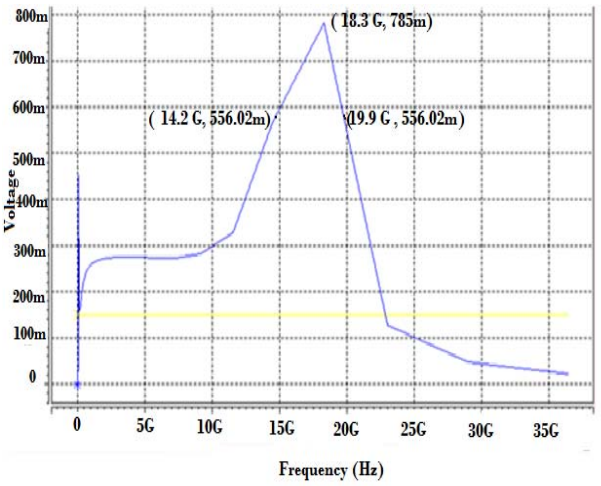

Fig. 4 Frequency response of output signal (deep blue) (values of cutoff frequencies are shown)

From the Fig. 4 , we get two -3 dB cutoff frequencies of our LNA circuit . These two frequencies are 14.2 GHz and 19.9 GHz. So,

-3 dB bandwidth = (19.9 - 14.2) GHz
= 5.7 GHz

C. Power Consumption

Power consumption is an important parameter of our LNA circuit. Our target is to keep this value as small as possible.
The following curve is showing the power consumption of our LNA circuit .

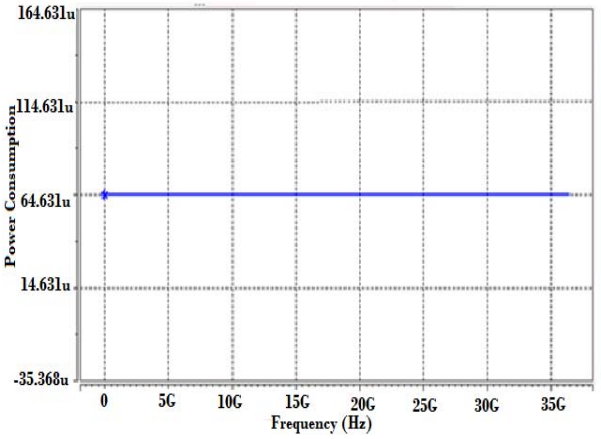

Fig. 5 Power consumption (deep blue straight line)

In Fig. 5 , power consumption is shown along Y-axis and unit is watt. Along X-axis frequency is shown in hertz. Power consumption of our proposed LNA circuit is 64.631 micro-watts.

V. CONCLUSION

This LNA circuit is designed to use in the medical application where low power consumption, high gain and ultra-wideband bandwidth are required. We have simulated our design in circuit level using rf_9 model in Hspice A-2008.03 Here, we have got very low power consumption, high gain and ultra wide bandwidth(bandwidth is more than 20% of centre frequency) from the simulation result.

ACKNOWLEDGMENT

This work was greatly supported by BUET central library providing different important books and giving a chance to get access to the different important papers on internet.

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