A Novel Folding Technique for 3 Bit Flash ADC in Nanoscale

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***Abstract*— In this paper we design and optimized the low power and high speed 3 bit flash Analog-to-Digital Converter (ADC) using 45 nm technology. For high speed application Resolution ,speed and power are optimized for implemented ADC.High integrated flash ADC is designed at three bit precision with operating voltage in range of 700 mV to 1V.This paper also describe the reduction in size of flash ADC and increase bit size of ADC using folding technique. Interpolation factor of 4 is introduced to reduce the comparators and resisters for generation of reference voltage. Interpolation technique reduces input capacitance, delay and increase the bandwidth of input signal .Lower leakage of 17.76 pW and high speed with minimum delay of 14.25 µs is achieved using folding technique .A noise of 0.86 µ dB and maximum SNR of 59 dB is reported in present paper .Folding and interpolation ADC is best suited for ultra low application.**

Keywords-Flash ADC;Folding;Interpolation;SNR;Noise.

I. Introduction

With the rapid incline of electronics system including communications and signal processing systems, ADC is the most popular components used in every consumer electronics and computer systems. In high speed and low power application flash ADC is used [1]–[4]. In recent years system –on-chip grows rapidly therefore signal processing component optimization is an important factor. Analog to digital converters (ADCs) is a mixed signal integrated a component that converts analog signals to digital signal; which is real world signals to digital signals for information processing component .Design of high speed, low operating voltage, low power consumption and the high input signal bandwidth analog-to-digital converter demand increasing rapidly [5]-[9]. Comparators are the important component of any flash ADC and performance ADC is strictly depending on comparators. Accurate and high precision of comparator is required for ADC performance optimization. Flash converters achieved better efficiency in 90 nm CMOS technology. [10] Compare with 0.18 nm [11] by cut down preamplifiers stage and fully depended on threshold calibration.Interpolation and folding [12] techniques achieves the higher resolution in compare with traditional flash technique but this technique work in the presence of preamplifiers .Both techniques have advantage to reduce power consumption in flash ADC. Preamplifiers include in interpolation technique or reducing the number of comparators in folding technique for particular resolution.

II. Flash ADC Architecture:

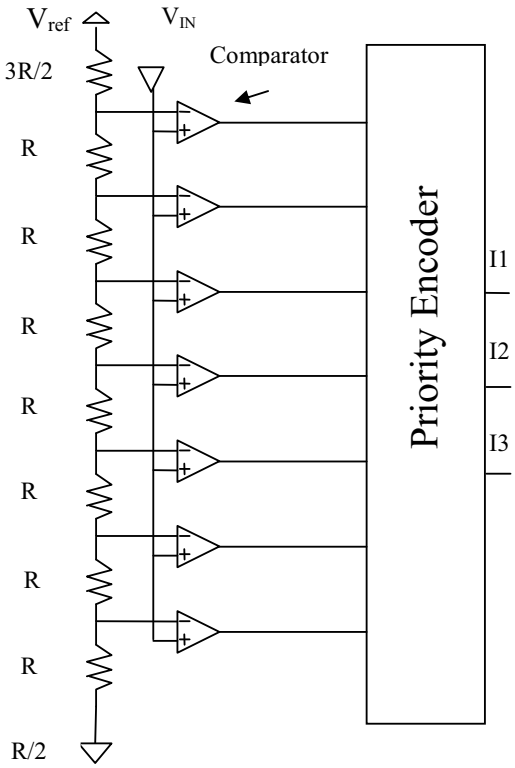

Figure1. Schematic of conventional flash ADC architecture

Figure 1 show block diagram of conventional flash ADC which is implemented using cadence virtuoso tool with 45 nm technology .Typical 3 bit flash converter is implemented here. Flash"3" bit converter, simply require 2^3-1= 7 comparators. A resistive divider that incorporated in converter employ 2^3 = 8 resisters requires for providing the reference voltage to comparators .The reference voltage provided by the resistive divider to each comparator is one LSB (least significant bit) that is higher than the reference voltage for the comparator just below it. Each comparator achieved the output "1" whenever input voltage source (analog) V_{IN} is higher than the reference voltage V_{ref} provided to comparators .The comparator give output "0"when analog input source is lower than reference voltage.

A. Resister divider section:

For 'n' bit flash ADC, double of n bit that is the 2n resistances is required .Each resistor having the same value R but two extreme position resisters are evaluated to

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delimit the input voltage range. Each resister in divider section divides the reference voltage that is applied in upper extreme resister to feed a comparator .Higher the resistance value then currently is consumed by the device become lower. That contributes the minimization of power dissipation in the device [13].

B. Comparator:

Flash ADC "n" bit architecture provides 2^n-1 comparators that consist of differential amplifier based. Each comparator achieved the output "1" whenever input voltage source (analog) V_{IN} is higher than the reference voltage V_{ref} provided to comparator. The comparator give output the "0"when analog input source is lower than reference voltage applied to it.

C. Priority encoder:

The output of the comparators is not in digital form ,but it is to be encoded. Therefore, a priority encoder is employed to convert the encoded signal into digital form means "n" bit data format that is binary code.An analog sinusoidal input of 5000 Hz with 700 mV is provided to flash ADC for determine the functionality of designed ADC .Fig 2 shows the Flash ADC transient output analysis of "3" bit flash ADC for analog input signal V_{SIN} of 5000 Hz frequency. Bit "0" represent the LSB and bit "2" represent the MSB of the binary digital output of "3" bit flash ADC.

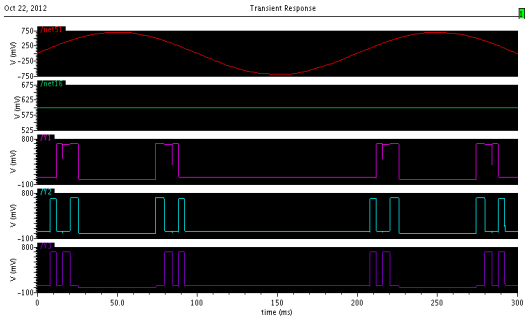

Figure 2.Transient behavior of flash ADC

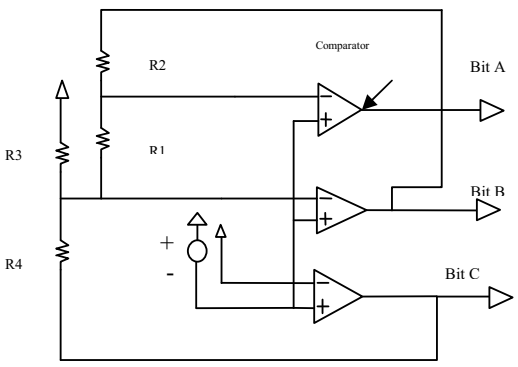

Figure 3.Schematic of folding technique architecture

III. Folding ADC Architecture

The optimization of ADC circuit is done by reducing the size of circuit which is the biggest disadvantage of flash ADCs. Therefore, folding technique is used to implement the logic circuit which requires the minimum number of comparators to increase bit size of ADC [14]. The number of comparators is required must below 2N by the employ of folding logic. Fig 3 shows the folding logic circuit that consists of different resisters which is connected to voltage source of 1 V generated "3" bit output .It employs only three comparators and reducing the size of flash ADC .Resisters value are chosen in such a way that "3" bit output are not overlapped .Different values of resisters must choose as R1=10K,R2=220K,R3=56 and R4=56K.Transient analysis of folding circuit is shown in fig 4.The output of folding circuit for given the sinusoidal wave Vsin of 700 mV amplitude and 5000 Hz frequency is shown below .The output of the folding ADC architecture has a higher frequency factor due to its input signal multiplies by folding factor thus reducing the size of ADC having biggest advantage of it.

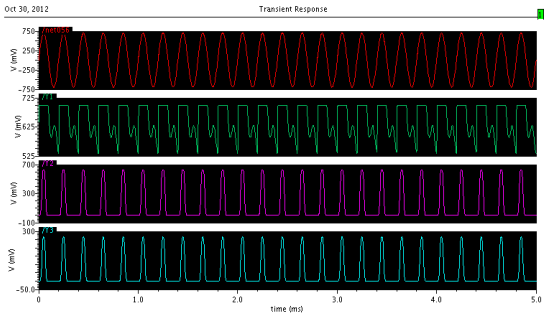

Figure 4. Transient behavior of ADC using folding technique

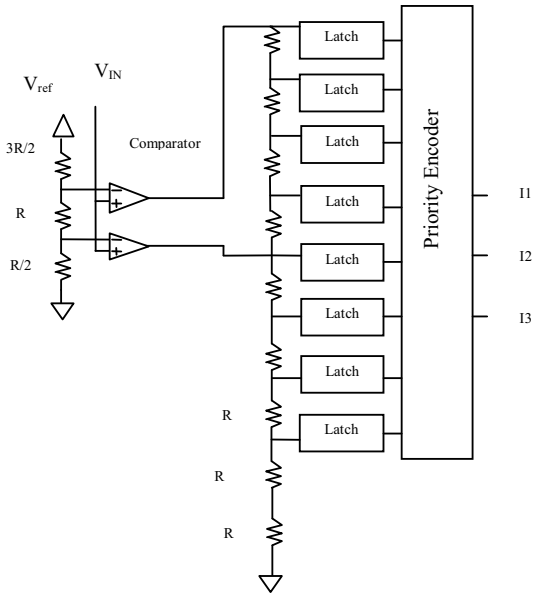

Figure5. Schematic of interpolation ADC

IV. Interpolation ADC Architecture.

The main drawback of flash ADC is the large number of comparators and resisters .Input capacitance increases and mismatch in resisters gene orate inconsistent output. Interpolation technique is used to reduce the number of comparators, resisters and reduce the reference voltage that is generated by resistive block .Fig 5 shows the block diagram of "3" bit interpolation architecture using the interpolating factor of 4.There are various methods to interpolate the input signal or folded signals, define as voltage-mode (resistive) interpolation and current-mode interpolation. The current mirror circuit basically based on current mirror. But current mirror produce non-idealities, therefore this method is not suitable. Here voltage mode interpolation is design using the resistive block and this block treat as passive interpolation that is used to generate intermediate voltages. The voltage-mode (resistive) interpolation can be designed by using a resistive ladder. Voltage-mode interpolation is better than other interpolation architecture and the low power operation.

V. Design of High speed Priority Encoder:

A priority encoder is an encoder that contains the seniority function. The performance of the priority encoder is such that whether two or more inputs are equal to one at the same time, the input having the stiffest priority will take preference. 8:3 priority encoders encode eight data lines to 3-bit binary data lines . This type of encoder is called the priority encoder [15] because it gives priority to the highest order input. In the priority encoder both input data lines and output data lines are active'' low''. An enable input and enable output also provides to the priority encoder, which allows octal expansion without any requirement of external circuitry. They enable input must be assumed to low state to enable the chip whereas they enable output goes to low state only when all inputs are inactive.

VI. Simulation and Performance Characteristics:

A .Power Simulation

Flash ADC and different techniques such as folding and interpolation is simulated by using cadence virtuoso tool with 45 nm technology. Here lower leakage power and average power consumption is observed for flash ADC using folding technique in comparison with interpolation and conventional flash ADC .Average power of 1.808×10^{-6} is consumed and Figure 8 shows the 17.76 pW instantaneous leakage power.

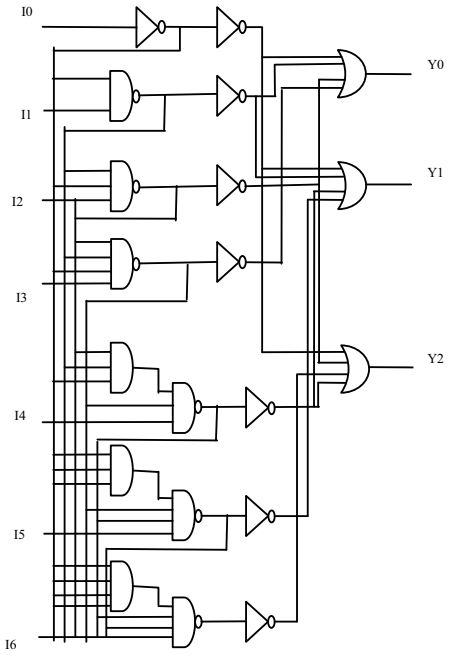

Figure6. Schematic of priority encoder

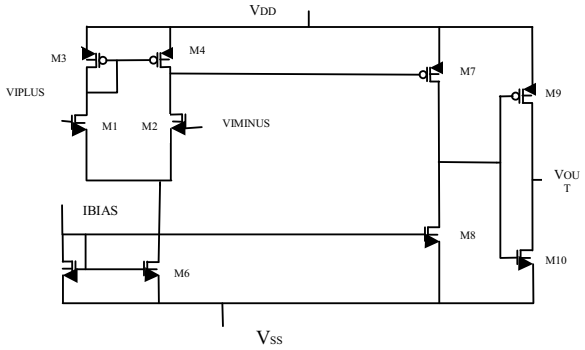

Figure 7.Schematic of comparator

B. Noise Simulation:

Resistor Noise Analysis:

Thermal noise is the dominant factor of noise that is generated by resistor divider section so here this type of noise is important one factor that affects the operation of different types of ADC .The series voltage generator can be described as noise source which is shown below.

$$V_R^2 = 4KTR_{eq.}\Delta F \quad (1)$$

Where K is the Boltzmann's constant, T is the room temperature, $R_{eq.}$ is the equivalent resistance,is the respective bandwidth at frequency of 5K Hz.

C. Coarse ADC Noise Analysis:

The Folding flash ADC is analyzed and simulated for noise calculation .At 5K Hz frequency, the folding flash

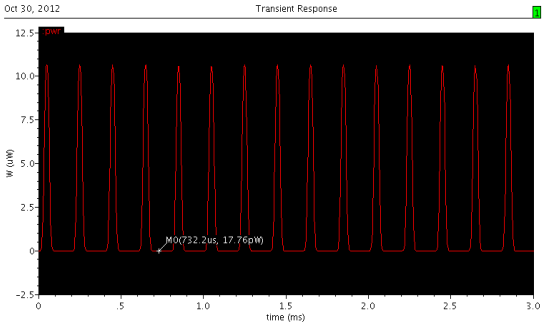

Fig8.Instantaneuos leakage power of flash ADC using folding technique

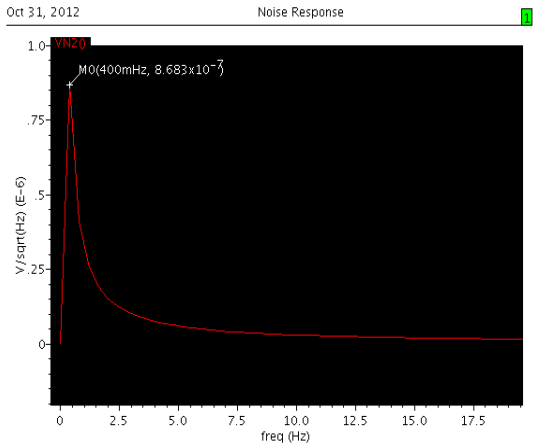

Figure9 Peak noise of flash ADC using folding technique

ADC generates a peak noise value of 8.683×10^{-7}. (V^2) at 400M Hz**.** Same noise analysis is performed for conventional and interpolation flash ADC .Minimum peak noise is calculated for folding ADC as compared with other two .Signal to noise ratio (SNR) [17] can be calculated with the help of peak amplitude of signal and noise .Peak noise is shown as in figure 9 and SNR can be calculated by given equation.

$$\text{SNR} = 20\log_{10}\left(\frac{A_{signal}}{A_{noise}}\right)\text{dB} \qquad (2)$$

Where A_{signal} and A_{noise} is the peak amplitude of signal and noise.

D. Frequency Jitter Simulation:

Input signal is periodically sampled as sampling theory play important role for data converters means ADC .If time duration between two samples of input signal is continuously constant the analog input will be exact replica of signal as corresponding digital signal at output .Jitter is deviation of time interval between two samples of signal with compared and measured with respect to the fixed time interval [18],[19].It may be defined as sampling errors that it degrade the signal at output of flash ADC .Jitter response on sampling of signal is defined by

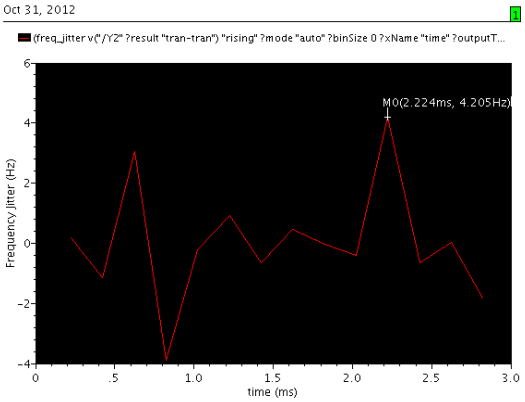

Fig 10.Frequency jitter of flash ADC using folding technique

voltage sampled error ($V_{err.}$) and it is calculated by equation is given below.

Here different types of ADC is analyzed and simulated at 45 nm technology using cadence virtuoso tool.Resolution of 3 bit is generated for all types of ADC .Lower leakage power 17.76 pW is observed that is lower than flash and interpolation type. Minimum period jitter value of 4 ms is generated for folding technique. Frequency jitter 4.02 Hz that is still minimum for ADC using folding technique as compared with other two type of ADC.

Table1.Output parameter Comparison of different ADC architecture

Parameters	Flash ADC	Folding ADC	Interpolation ADC
Technology	45 nm	45 nm	45 nm
Resolution	3 bit	3 bit	3 bit
Average power consumption	14.8 µW	1.808 µW	2.398 nW
Leakage power	45.04 µW	17.76 pW	120 µW
Period Jitter	182 ms	400.0 µW	200 ms
Frequency jitter	30.12 Hz	4.02 Hz	4.51G Hz
Delay	4.83 ms	14.25 µs	65 ps
Signal to noise ratio (SNR)	56.36 dB	59 dB	56.75 dB
SNHR	5.817dB	189.4dB	164.6
ENOB	3.45-bit	1.543-bit	1.538-bit
SFDR	5.967dB	13.07dB	13.07dB

Conclusion:

This paper demonstrates the various ADC architecture and explore the various performance characteristics of different flash ADC. A "3" bit flash ADC and high speed interpolation ADC has been designed for ultra low power application in 45 nm CMOS technology .A folding technique is applied to reduce the size and leakage in flash ADC .Folding technique reduces size of converter by decreasing number of comparators that enhance and optimized the various characteristics of converter .Low resolution of 3 bit, lower leakage power of 17.76 pW, is achieved by implementing folding technique .Interpolation and folding ADC is designed using cadence tool in 45 nm technology .Reduction in reference voltage is observed by using interpolation technique that introduce interpolation factor of 4.

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