Comparative analysis of Schmitt trigger with AVL (AVLG and AVLS) technique using nanoscale CMOS technology

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***Abstract*—The CMOS device is used to achieve better performance in terms of speed, power dissipation, size, reliability and hysteresis. Schmitt trigger minimized power consumption and improving compatibility with low voltage power supplies and analog component the most effective solution is to reduce the power consumption. This paper presented comparative study of AVLG, AVLS and AVL technique in 4T Schmitt trigger is used in such a way that by adjusting its threshold voltage, the signal can be made to increase early, thereby reducing the signal delay also due to less switching time, power dissipation is less, circuit is simulated in cadence in 45nm technology, simulation results show that 4T Schmitt trigger delay reduction 102.8ns at 1V and 3.97fw leakage power reduction at 0.7V input supply with AVL technique.**

Keywords-Schmitt trigger; AVL; Delay; Power dissipation; Efficiency.

I. INTRODUCTION

Digital circuit does not directly suitable for defining the digital signal, for some reasons it may have slow rise or fall time and may have the small noise sense by proceeding circuitry, so all of these critical conditions required a specified device that will "clean up" or maintain a signal the required device is known as the Schmitt trigger [1], output state depends on input state and changes only as input level crosses a preset threshold level. Schmitt trigger device is mostly used in analog and digital (0 or 1) circuit as wave shaping device to resolve the noise problem [2], This device is widely used to drive the load with fast switching low power loss and low power supply [3]. Schmitt trigger has been used irrelevant to improve on/off (0 or 1) control state [4], and reduce the sensitivity to noise, for example, sensor [3], pulse with modulation circuit [6]; SRAM [8][9], Schmitt trigger is the decision making circuit. Schmitt trigger is used to convert a slowly varying analog signal voltage into possible binary states, depending on the analog voltage is above or below a predefined (preset) threshold voltage. Schmitt trigger can act as a signal restoring circuit; this is the main reason why we have looked into the approach of using Schmitt trigger as an alternate of buffer in interconnects as a data restoring element. The conventional Schmitt trigger circuit with different [1 to 0] and [0 to 1] transition threshold voltage (VH and VL) has better noise sensitive than the inverter [10], when the input signal goes to vdd to gnd, threshold voltage of the Schmitt trigger circuit is (VH) and when the input signal in goes down to gnd from vdd, the threshold voltage of the conventional Schmitt trigger is VL [15][16], The main difference between Schmitt trigger and comparators shows by DC transfer characteristics. Comparator show one switching threshold, besides Schmitt trigger shows difference switching threshold value for positive edge and negative edge input signal, this type of property is called hysteresis [16]; The Schmitt trigger is comparator that has positive feedback [5]. It reduced the power consumption (dynamic and static) by using AVLG, AVLS, and both (AVLG & AVLS) simultaneously in 45nm technology is the main goal of presented paper.

II. CIRCUIT DESCRIPTION

A. 4T Schmitt Trigger

The proposed circuit is formed by a combination of one PMOS (P1) and three NMOS (N1, N2 and N3), there is no direct connection between power supply and ground as PMOS is connected to power supply and circuit output, beside NMOS is connected to output and ground node, there is no static power due to no direct connection between power supply to be ground. Hysteresis of the Schmitt trigger is defined as.

$$\Delta H = V_H - V_L \tag{1}$$

The Schmitt trigger is implemented by PMOS and NMOS sub circuit. PMOS device is formed with two doped p+ regions known as drain and source and are separated by distance L .the interface between drain and source terminals known as gate and separated by silicon dioxide material. NMOS device is formed by two N+ regions within a lightly doped p substrate. PMOS and NMOS work in mainly in three regions, which are defined as.

$$I_D = 0(off: |V_{GS}| < |V_{TH}|) \tag{2}$$

$$I_D = k * \left(\frac{W}{L}\right)\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right](triode: |V_{DS}| \leq |V_{GS}| - |V_{TH}|) \tag{3}$$

$$I_D = \left(\frac{k}{2}\right) * \left(\frac{W}{L}\right) * (V_{GS} - V_{TH})^2 * (1 + \lambda_{n,p}V_{DS})(saturation: |V_{DS}| \geq |V_{GS}| - |V_{TH}|) \tag{4}$$

We have following regional relation

$$NMOS\begin{cases} V_{out} > V_{DD} - V_{Tn}: off \\ V_{in} \leq V_{DD} - V_{Tn}: triode \\ V_{in} \geq V_{DD} - V_{Tn}: saturation \end{cases} \tag{5}$$

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$$PMOS\begin{cases} V_{in} < -V_{Tp}: off \\ V_{out} \geq -V_{Tp}: triode \\ V_{out} \leq -V_{Tp}: saturation \end{cases} \quad (6)$$

In above equation V_{GS}= gate to source voltage, V_{DS}= drain to source voltage, V_{TH}= threshold voltage.

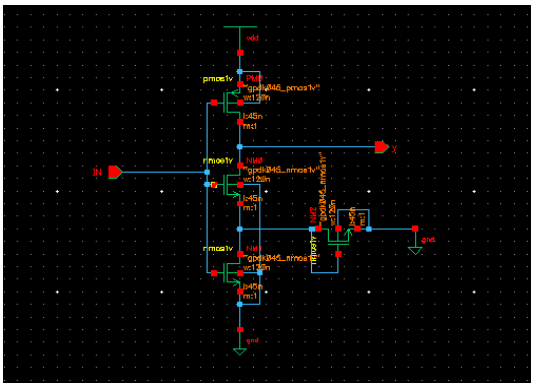

Figure 1 Circuit diagram of the 4T Schmitt trigger.

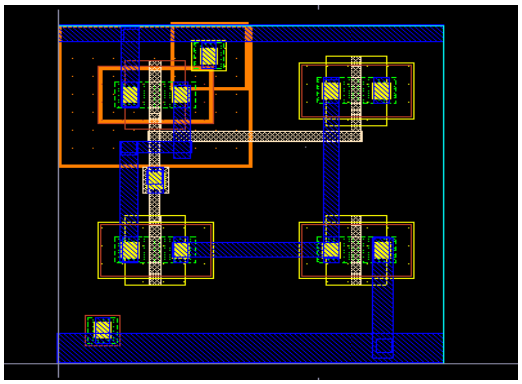

Figure 2 Layout of the 4T Schmitt trigger.

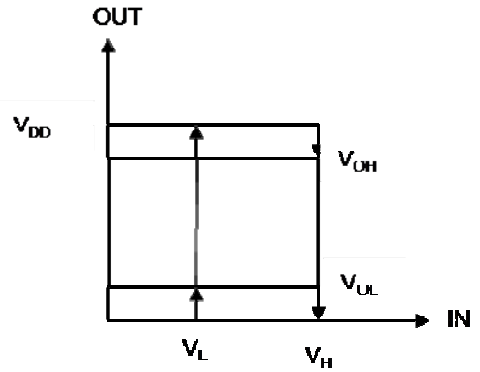

Figure 3 The transfer curve of the 4T Schmitt trigger.

Figure 1 shows the 4T Schmitt trigger with one PMOS and three NMOS circuit to be reduced mainly delay of the circuit where Vdd=0.7v power supply and Vin = (0.7v to 1v). Figure 2 show the layout of 4T Schmitt trigger And Figure 3 shows the input –output waveform of the Schmitt trigger. It is also known as the hysteresis plot.

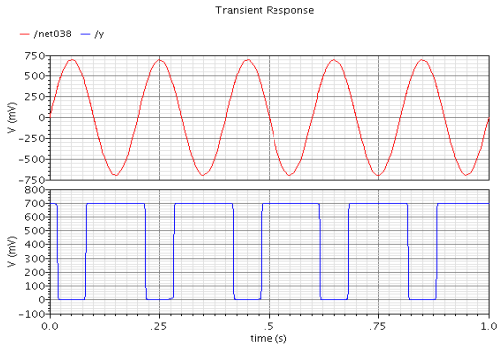

Figure 4 The input-output characteristic of the 4T Schmitt trigger.

Figure 4 shows waveform the transfer characteristic of the 4T Schmitt trigger at 0.7v power supply.

B. *Adaptive Voltage Level (AVL)*

1) *Control Circuit*

An adaptive voltage level control circuit [6] can be used either at the upper end of the cell to reduce supply voltage (AVLS scheme) or at the lower end of the cell to raise the potential of the ground node (AVLG scheme). The impact of these two techniques on leakage currents is described in this section.

2) *AVLG technique in schmitt trigger*

Fig.5 it shows a schematic of a 4T Schmitt trigger in which AVLG scheme is applied. The switch provides zero volts at the ground node during the active mode and a raised ground level (virtual ground) during the inactive mode. This scheme is similar to the diode footed cache design scheme proposed to control gate and sub-threshold leakages in Schmitt trigger, in which a diode designed with high Vt MOS transistors, was used to raise the ground level of the Schmitt trigger in the inactive mode.

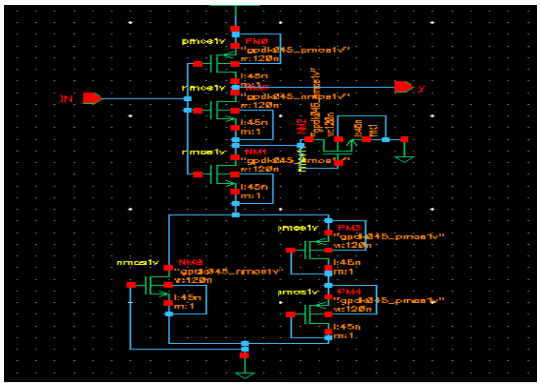

Figure 5 4T Schmitt trigger using AVLG technique.

Figure 5 shows the AVLG technique in the 4T Schmitt trigger in 45nm technology.

3) *AVLS technique in Schmitt trigger*

AVLS scheme has a better impact on gate leakage current reduction than the AVLG scheme. To summarize, the AVLS approaches, while more successful in reducing the gate leakage current, still leaves two gate leakage current components in access transistors unaltered. It too

leaves one sub-threshold current component in access transistor unchanged and results in an additional sub-threshold leakage current across the other access transistor.

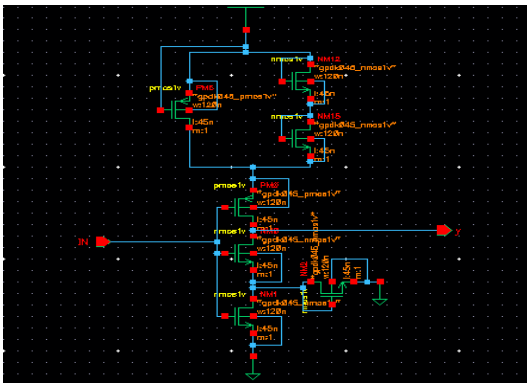

Figure 6 4T Schmitt trigger using AVLS technique.

Figure 6 shows the circuit, a diagram shows the AVLS technique with 4T Schmitt trigger and provides better performance in comparison to AVLG technique in 45nm technology.

4) AVL (AVLG & AVLS)

AVL technique provides AVLS (Adaptive Voltage Level supply) and AVLG (Adaptive Voltage Level ground) technique and provides a better result in comparison to individual AVLG and AVLS technique. In AVL technique, AVLG circuit applied at the top of the Schmitt trigger circuit and AVLG circuit applied at bottom of the Schmitt trigger and improved the performance of the device.

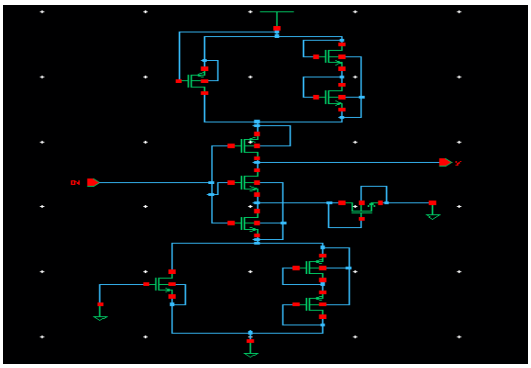

Figure 7 4T Schmitt trigger using AVL(AVLS & AVLG)technique.

Figure 7 shows the 4T Schmitt trigger with the AVL (AVLG & AVLS) techniques at different input voltage (Vin = 0.7 to 1v) at Vdd= 0.7v.

III. SIMULATION RESULT

Simulation results are simulated on the 45nm cadence tool with a nominal supply voltage 0.7 volt. The gate leakage being the only dominant mechanism at room temperature, AVLG method suppresses the total leakage of 4T is 13.91fw, while AVLS scheme provides a leakage reduction of 10.86 % and propagation delay in AVLS is 328.5ns better than AVLG technique and provide 64.68 % efficiency in AVLS. When we applied both AVLG and AVLS technique simultaneously then Schmitt trigger provided the best result in terms of power, delay, and efficiency.

A. Power analysis

For a CMOS circuit, the total power dissipation includes dynamic and static components during the active mode of operation. In standby mode, the power dissipation is due to the standby leakage current. Dynamic power consumption consists of two components. One is the switching control due to charging and discharging of load capacitance [22]. The other short circuit power is due to the nonzero rise and fall time of input waveforms. The static power of a CMOS circuit is finding by the leakage current through each transistor. Average power Pavg, the dynamic (switching) power P_D and leakage powerP_{LEAK} are expressed as.

$$P_{avg} = V_{dd}.I_{avg} = V_{dd}.I_{dd} \quad (7)$$

$$P_D = \propto fCV_{dd}^2 \quad (8)$$

$$P_{LEAK} = I_{LEAK}.V_{dd} \quad (9)$$

Where α is the switching activity; f is the operation frequency; C is the load capacitance; Vdd is the supply voltage; Idd is drain current Leakage power in Schmitt trigger using AVLS technique (10.86fw) provide a better result than AVLG technique (13.91fw).

Static and dynamic power in AVLG technique = (17.78fw and 83.62pw) at 0.8v (10)

Static and dynamic in AVLS technique= (13.70fw and 82.1pw) at 0.8v (11)

Static Power reduction in Schmitt trigger =21.9 % at 0.7V (11)

Dynamic power reduction in Schmitt trigger=16.98 % at 0.7V (12)

In Schmitt trigger AVLG and AVLS technique both applied simultaneously provide leakage power and dynamic power (3.97fw and38.02pw) respectively at 0.7v supply voltage.

TABLE I. STATIC POWER ANALYSIS

Voltage	Static power dissipation with AVLG	Static power dissipation with AVLG	Static power dissipation with Both (AVLS & AVLS)
0.7V	13.91fW	10.86fW	3.97fW
0.8V	17.78fW	13.70fW	4.34fW
0.9V	22.39fW	17.02fW	4.67fW
1V	27.96fW	20.89fW	4.99fW

Table I shows the power parameter of the Schmitt trigger in 45nm technology with AVLG, AVLS, and AVL (AVLS and AVLG) technique.

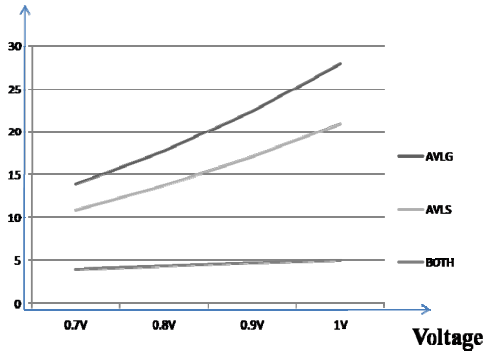

Figure 8 Static power analysis.

Figure 8 shows the graph of static (leakage) power analysis in the 4T Schmitt trigger in different technique (AVLG, AVLS, AVL) at Vdd=0.7v and AVL (AVLG & AVLS) provide less static power dissipation.

TABLE II. DYANEMIC POWER ANALYSIS

Voltage	Dynamic Power		
	AVLG	*AVLS*	*Both (AVLG & AVLS)*
0.7V	83.62pW	69.41pW	38.02pW
0.8V	86.53pW	82.1pW	61.14pW
0.9V	124.5pW	117.8pW	116.1pW
1V	189.6pW	139.4pW	112.4pW

Table II shows the AVL technique provides the best result in static and dynamic power at input voltage (0.7v to 1v) in comparison to AVLG, AVLS and both (AVLG & AVLS) technique.

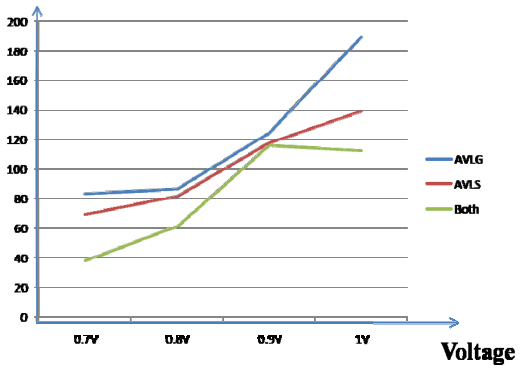

Figure 9 Dynamic power analysis.

Figure 9 shows the graph of dynamic power analysis in the 4T Schmitt trigger at different input voltage (Vin = 0.7to 1v).using AVL technique dynamic power is reduced up to 16.9%.

B. Delay

Schmitt trigger as an alternate to buffer to reduce delay and power in interconnects is examined. The most positive feature of Schmitt trigger is its adjustable threshold voltage, and it can be controlled, the threshold voltage can be selected to be above or below$V_{dd}/2$, a voltage at which buffer normally operates.

Thus a Schmitt trigger can be designed to switch faster than a buffer leading to a reduction in delay. The adjustable low-voltage threshold of the Schmitt trigger handles more noise and voltage glitches as compared to buffer [13]. The time taken for a Schmitt trigger logic gate output to change after one or more inputs have changed is known as delay [7]. The simulation Results observes that AVLS with Schmitt trigger gives a better performance as compared to AVLG and less delay (328.5ns) in 45nm technology.

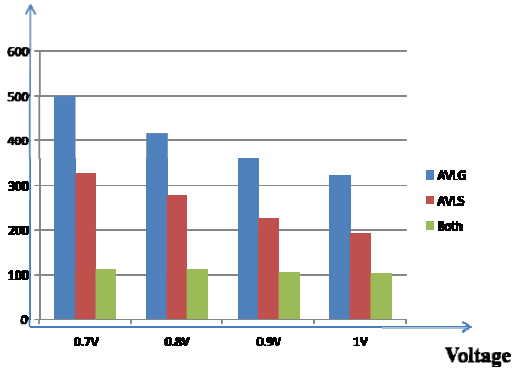

Figure 10 Delay analysis at different technique.

Propagation delay reduction = 34.16 % (13)

The Delay of the through during a signal transition is given as;

$$\text{Delay} = 0.69R_{eq} * C_L \quad (14)$$

Where in above equation $R_{eq}$is the resistance that is implemented using the feed through cell and C_L is the load capacitance.

Delay in Schmitt trigger using the AVL (both AVLG and AVLS) techniques is 112.8ns at supply voltage (Vdd=0.7v)

TABLE III. PROPAGATION DELAY ANALYSIS

Voltage	Propagation Delay		
	AVLG	*AVLS*	*Both (AVLG & AVLS)*
0.7V	499.0nsec.	328.5nsec.	112.8nsec.
0.8V	416.5nsec.	276.4nsec.	110.6nsec.
0.9V	361.0nsec.	224.5nsec.	104.6nsec.
1V	321.1nsec.	192.5nsec.	102.8nsec.

Table III shows, the propagation delays analysis in AVLG, AVLS and AVL (AVLG and AVLS) and lesser delay provided by AVL technique (112.8ns) at (Vin= 0.7v).

Figure 10 shows the delay analysis and provides the best delay in AVL technique at power supply (Vdd=0.7v).

C. Efficiency

Efficiency= (output value/input value)*100 (15)

It is denoted with Greek letter. Efficiency cannot be more than 100%.High High efficiency means fewer power drains and the input source and fewer heat buildups,

allowing for smaller lighter power supplies and system enclosures. The highest possible efficiency is desired when battery life is critical and when package size restrictions preclude effective heat removal.

Schmitt trigger provides best efficiency with AVL (both AVLG and AVLS) (76.84%) in comparison to single AVLG and AVLS technique.

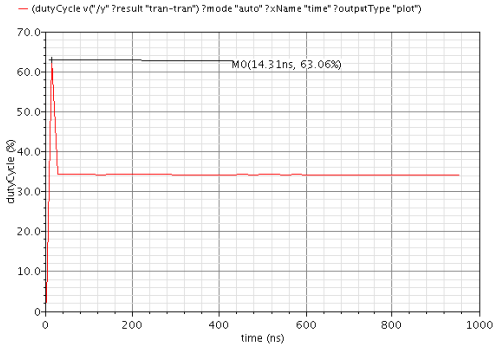

Figure 11 Efficiency analysis in AVLG technique.

Figure 11 Shows the waveform shows the circuit efficiency in the 4T Schmitt trigger with AVLG technique at Vdd=0.7v.

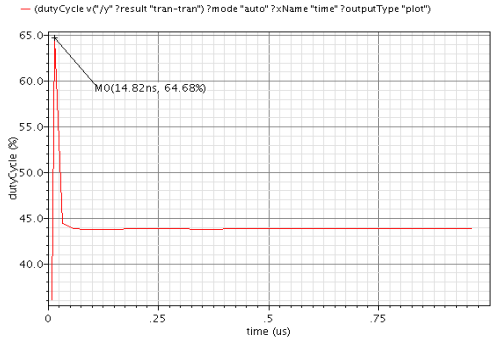

Figure 12 Efficiency analysis in AVLS technique.

Figure 12 shows the overall efficiency of the 4T Schmitt trigger (64.68%) with AVLS technique.

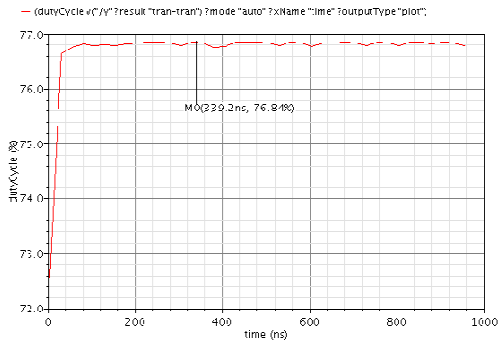

Figure 13 Efficiency analysis in AVL technique.

Figure 13 Shows the waveform of efficiency of the 4T Schmitt trigger with AVL (AVLG & AVLS) (76.84%) and provides best circuit efficiency in comparison to AVLG and AVLS technique.

IV. CONCLUSION

4T Schmitt trigger is developed using cadence IC design environment in 45nm technology. AVLG, AVLS and AVL (AVLS & AVLG) techniques have been used in presented work. An AVL (adaptive voltage level) technique Schmitt trigger is proposed offers reduced gate and threshold leakage power. Simulation result show that 21.9% reduction in static power and 16.9% reduction in dynamic power at 27·c provides by AVL technique using both AVLG and AVLS circuit AVLG technique achieved 63.06% circuit efficiency AVLS(64.68%), on other hands both AVLG & AVLS technique (76.84%) improved overall efficiency. Schmitt trigger, measured result correctly verified the principle of operation and characteristic of the low-power Schmitt trigger circuit. The circuit has been used for the design of low power.

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