Optimization of Leakage Current in SRAM Cell Using Shorted Gate DG FinFET

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***Abstract*— Scaling of conventional CMOS circuit tends to have short channel effects due to which, effect such as drain induced barrier lowering, hot electron effect, punch through etc takes place and hence leakage increases in the transistor. To minimize short channel effects, double gate FinFET is used. FinFET may be the most promising device in the LSI (large scale integration) circuits because it realizes the self-aligned double-gate structure easily. In this paper, six transistors SRAM cell is designed using the tied gate DG FinFET. Sub-threshold leakage current and gate leakage current of internal transistors are observed and compared with the conventional structure of 6T SRAM cell. DG FinFET SRAM cell is applied with self controllable voltage level technique and then leakage current is observed. Simulation is performed with cadence virtuoso tool in 45 nm technology. The total leakage of DG FinFET SRAM cell is reduced by 34% after applying self controllable voltage level technique.**

Keywords- CMOS, SRAM cell, tied gate DG FinFET, leakage current.

I. INTRODUCTION

The CMOS scaling of the devices is facing challenges due to shrinking geometries, lower supply voltage, and higher frequencies, this have negative impact on the device by increasing short channel effect due to which leakage (gate leakage and sub-threshold leakage) in the device is increasing constantly [1]. High V_{dd} and high V_t improves SNM (Static noise margin) results in data stability during read operation [2] however as the V_{dd} increases so does the power consumption. Process induced variations and sub-threshold leakage in bulk Si technology is more as compared to SOI devices. Multi-gate devices would result good impact on the digital circuits as they provides better electrostatic control in the device. The multi-gate FinFET devices can be used in fabricating double gate, tri-gate and quasi-planar all around (QAA). The paper here describes SRAM cell using double gate (DG) FinFET [3] and highlights the important improvement in terms of leakage power consumption as compared to conventional MOSFET based SRAM. Double gate FinFET may be employed using various design types as shorted gate (SG) and independent gate (IG) [4]. Here we would analyze the SRAM cell using SG Double Gate FinFET and compare the results with the conventional SRAM cell for leakage and power performance. The two gates on either side can be tied together which switches the FinFET ON or OFF. Double gate FinFET has good cut-off characteristics and greater scalability [5]. Basically, FinFET is designed with a thin fin which serves as a body and helps in conduction and reduces SCE [6][7]. Therefore double gate FinFET is used to reduce short channel effect. Moreover, when larger circuits are used, difference between the bulk CMOS and FinFET appears [8]. FinFET is also divided into bulk FinFET and SOI FinFET. Bulk FinFET is designed with high doping and have disadvantage of SCE for short channel length [9]. Therefore silicon on insulator FinFET is largely preferred.

The organization of the paper is as follows: Section 2 describes the operation of conventional SRAM cell. Section 3 describes the operation of DG FinFET SRAM. Section 4 describes leakage in both conventional SRAM and DG FinFET SRAM. Section 5 describes leakage control in both. Section 6 shows simulation results and section 7 concludes the paper.

II. OPERATION OF CONVENTIONAL 6T SRAM CELL

In the given SRAM cell, six transistors are used in which four transistors (two PMOS and two NMOS) form a latch and two NMOS are the pass transistors. The two PMOS (M1 and M2) and two NMOS (M3 and M4) form two inverters which are connected back to back. The other NMOS transistors (M5 and M6) are the access transistors which are enabled through write line (WL). The two bit lines are used for read and write operations [10]. Data is stored in cross coupled inverters. The structure is shown in Fig.1.

The read and write operation depends on the WL and two bit lines BL and BLB. For the period in which WL is at high (say, Vdd= 0.7 V), the NMOS transistors M5 and M6 becomes 'ON' and allow access to the storage nodes 'Q' and 'QB'. For the write operation, both the bit lines are at opposite voltages i.e. if bit line BL is high, then bit line BLB will be it's complement. In the operation of given 6T SRAM cell, both bit lines are kept at opposite voltages (BL=1, BLB=0 or BL=0,BLB=1) and when WL enables transistors M5 and M6, the data writes on the nodes Q and QB of back to back connected inverters. Similarly, read operation of SRAM cell is inverted of the write operation. For read operation, both bit lines are at high voltage, and WL is raised to high. Since one of the nodes is low, one of the pre-charged

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bit lines start discharging and at that instant data can be read at the time of discharging. A sense amplifier is connected to the output node to read the changing value. Therefore read and write cycle is performed. The waveform is shown in Fig.2.

According to the drawn waveform, the period in which WL is at 0.7 V, write operation takes place, output Q depends on BL and QB depends on BLB. When WL is 0 V, the device becomes in standby mode i.e. it is neither read nor written. The delay in the write operation is about 138 ps and that of read operation is 110 ps.

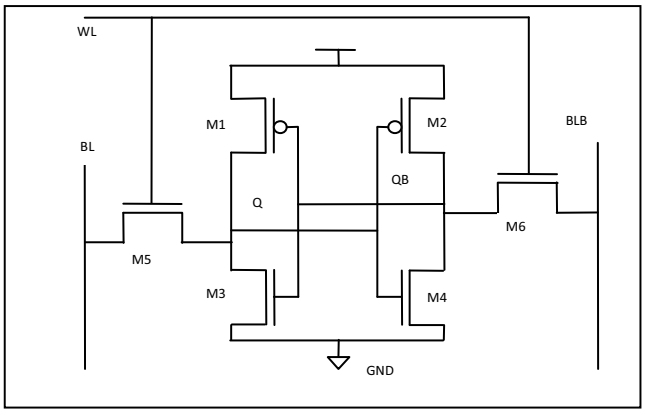

Figure 1. Schematic of conventional 6T SRAM cell

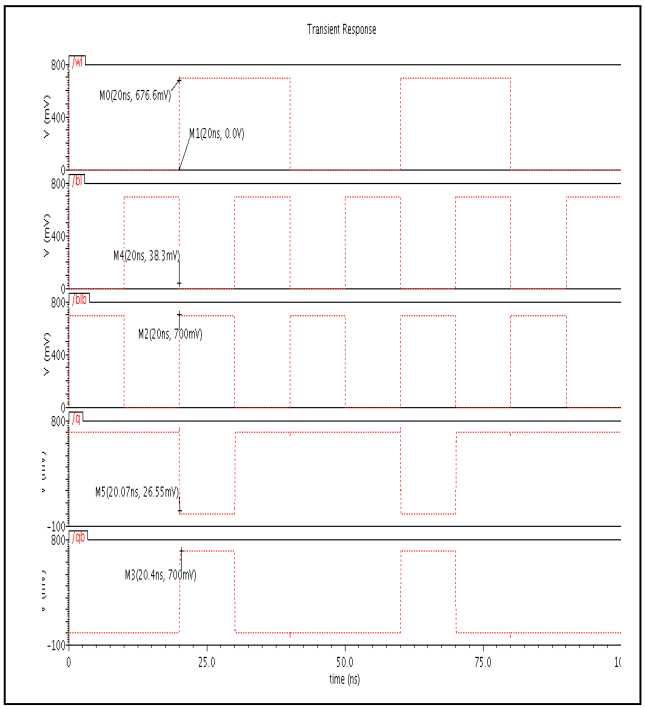

Figure 2. Waveform of operation of SRAM cell.

III. 6T SRAM CELL USING DOUBLE GATE FINFET

The shorted gate DG FinFET SRAM cell structure is superior choice due to the self-alignment of both gates and the fabrication compatibility with the existing standard CMOS fabrication technology [11]. It also consists of WL to enable access FinFET NMOS transistors. Two DG FinFET inverters are connected back to back same as the bulk CMOS SRAM. FinFET reduces the SCE and hence leakage, but delay in the 6T SRAM is increased by using DG FinFET to some extent during the operation. The structure of 6T SRAM designed by double gate is shown in Fig. 4.

The operation of DG FinFET SRAM is same as the conventional SRAM but the delay increases because the time of switching of output waveform increases. Leakage current here has been reduced to a significant level as compared to the conventional SRAM cell.

The structure of 6T SRAM cell using DG FinFET is shown in fig.3.

IV. LEAKAGE CURRENT IN THE CELL

Sub-threshold leakage is the drain source current of the transistor when the gate source voltage is less than the threshold voltage (Vgs < Vth) [12]. In the weak inversion (or sub-threshold) regime, the drain current depends exponentially on the gate-source voltage given by equation (1).

$$I_d \propto \exp\left(\frac{V_{gs}}{nV_T}\right) \quad (1)$$

where, $$V_T = \frac{kT}{q}$$

V_T is the temperature voltage with k being the Boltzmann constant, T is the absolute temperature, and q is the electron charge.

Gate current is the leakage current that flows when the transistor is OFF. Since oxide scaling increases the field across the oxide. The high electric field coupled with the low oxide thickness results in gate tunnelling leakage current from the gate to the channel and source/drain overlap region, or from the source/drain overlap region to the gate.

In both 6T SRAM cell, the bit lines are at V_{dd} and WL is low during standby mode. During standby mode, when low voltage is stored, NMOS transistors will have gate leakage. As sub-threshold current produces in OFF state transistor, transistor M3 and M2 will have sub-threshold leakage .Fig.4 and Fig.5 show the waveforms of conventional 6T SRAM cell and DG FinFET 6T SRAM cell.

V. PROPOSED WORK

In the proposed work, self controllable voltage technique [13] is applied on the shorted gate DG FinFET SRAM cell to further reduce the leakage in the cell. A circuit containing two NMOS transistors connected in series and a PMOS connected parallel to those two NMOS transistors, is connected below which provides ground during active mode and an increased ground voltage (virtual ground) during standby mode. Another circuit consisting of two PMOS transistors connected in series and a NMOS connected parallel to those two PMOS transistors, is connected above

the SRAM cell which provides a full supply voltage in active mode and voltage level is reduced at standby mode. Both circuits connected at upper end and lower end of the shorted gate DG FinFET SRAM are termed as USVL (upper SVL) and LSVL (lower SVL) respectively which together provides the reduced leakage to the FinFET SRAM cell. The operation of SVL can be easily understood using CMOS inverter as shown in fig.6. When "clk=1" and "clkbar =1" Thus, the USVL and LSVL circuits respectively generate a slightly lower supply voltage and a relatively higher "ground-level" therefore the leakage in off transistor reduces. Similarly, this technique reduces the leakage current in the shorted gate DG FinFET SRAM cell.

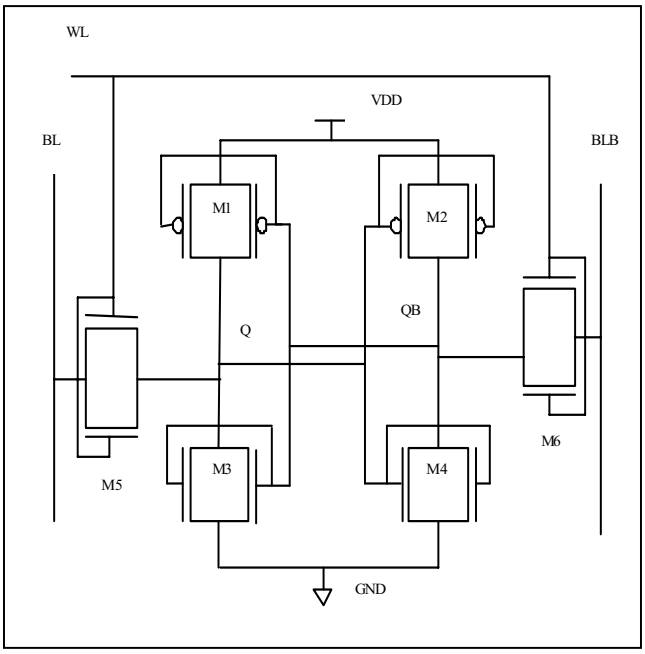

Figure 3. Schematic of DG FinFET 6T SRAM

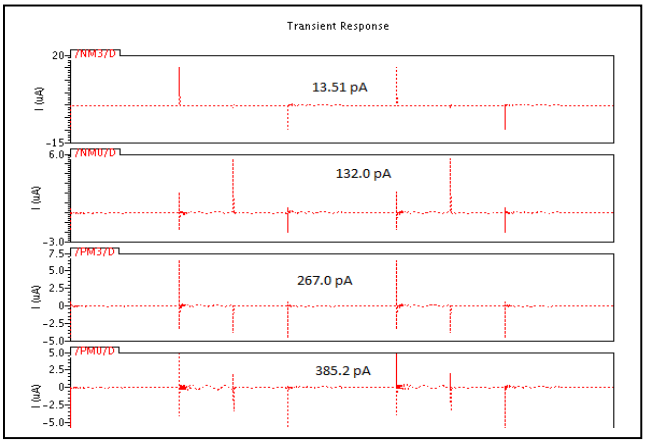

Figure 4. Waveform of leakage current in conventional 6T SRAM Cell

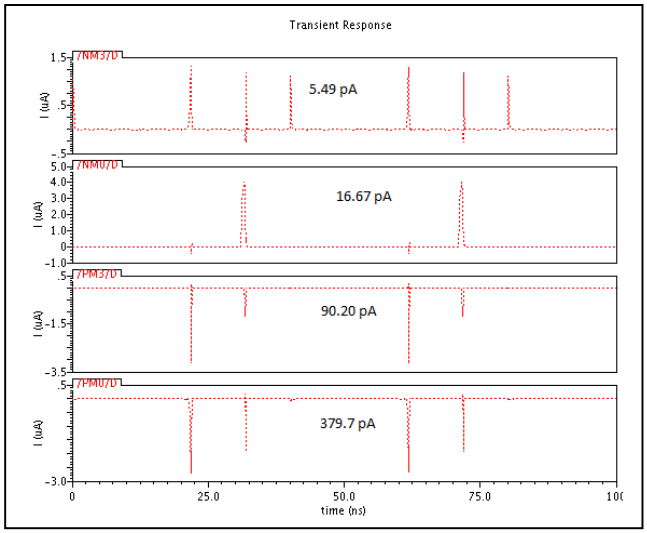

Figure 5. Waveform of leakage current in 6T double gate FinFET SRAM cell at 0.7 V

VI. SIMULATION RESULTS

The simulation of 6T SRAM cell and DG FinFET 6T SRAM cell is performed. Various parameters like length and width of transistor, temperature affect the circuit. The simulation is performed at 27^{o} C, channel length 45 nm and width 120 nm. Small amount of delay is increased in shorted gate DG FinFET but the leakage current in conventional SRAM cell is 869.9 pA and that of DG SRAM is 88.0 pA. Then SVL technique is applied on the DG SRAM cell which reduces the leakage current of SRAM cell to 301.02 fA. Table 1 shows the result of comparison of leakage current in conventional and shorted gate DG FINFET 6T SRAM cell and Table 2 shows comparison of leakage current in SRAM cell after implementation of SVL circuit.

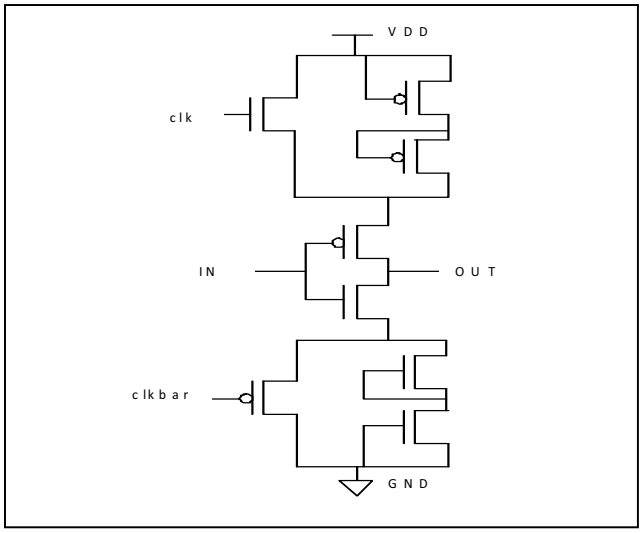

Figure 6. Schematic diagram of inverter showing implementation of SVL technique

TABLE I. COMPARISON OF LEAKAGE CURRENT IN CONVENTIONAL AND DG FINFET 6T SRAM CELL AT V_{DD} = 0.7 V.

6T SRAM CEL	M1		M2		M3		M4		Total leakage
	Igate (pA)	Isub (pA)	Igate (pA)	Isub (pA)	Igate (pA)	Isub (pA)	Igate (pA)	Isub (pA)	(pA)
Conventional	344.0	385.2	136.6	267.0	171.2	132.0	315.0	13.51	869.9
Double Gate FinFET	16.84	379.7	1.69	90.20	2.29	16.67	2.19	5.49	88.0

TABLE II. COMPARISON OF LEAKAGE CURRENT IN SRAM CELL.

SRAM cell	Leakage current
Conventional	869.90 pA
Shorted gate DG FinFET	88.00 pA
Shorted gate DG FinFET with SVL	301.02 fA

VII. CONCLUSION

Conventional 6T SRAM and DG FinFET 6T SRAM are analyzed through cadence virtuoso tool in 45 nm technology. It is seen that sub-threshold and gate leakage, both effects the operation of the SRAM cell. In this paper sorted or tied double gate FinFET is used to simulate the 6T SRAM cell and it is concluded that DG FinFET increases the performance of SRAM cell. The considerable change in the sub-threshold leakage is observed in comparison with the gate leakage. Total leakage in the SRAM cell can be reduced to 10 % using double gate FinFET. Further SVL technique is applied in shorted gate DG FinFET SRAM cell in which LSVL provides increased ground voltage and USVL provides reduced supply voltage during standby mode which reduces the leakage by 34 %.Therefore, results in reduced power dissipation and increased performance.

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