Leakage Minimization of 10T Full Adder Using Deep Sub-Micron Technique

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Abstract:
In this paper we introduced low leakage 10T one-bit full adders cells are proposed for mobile applications. The analysis has been performed on various process and circuits techniques, the analysis with leakage power. We introduced a new transistor resizing approach for 1bit full adder cells to determine the optimal sleep transistor size which reduce the leakage power and area to minimize leakage current. We have performed simulations using Cadence Virtuoso 45nm standard CMOS technology at room temperature with supply voltage of 0.71V. Simulations have been also compared for multiple V_{DD}. Thus design guide-lines have been derived to select the most suitable topology for the design features required. This paper also proposes a novel figure of merit to realistically compare 1-bit adders implemented as a chain of one-bit full adders. The CMOS leakage current at the process level can be decreased by some implement on deep sub micron method. The circuit level technique is reduced power consumption at very high level. In this paper we simulate the 10T Adder using many techniques both circuit level, process level.

Key Word —Adder, CMOS, MOSFET Transistor Leakage and Threshold Voltage

I. Introduction:

Due to increasing the demand of low power ICs for digital Circuits, use in like palmtop computers, cellular mobile, etc design choices which take into consideration low power features along with other circuit features like speed, area, performance life time, accuracy etc. Additions are heart of computational circuits and many complex arithmetic circuits are based on the addition and it is often one of the speed-limiting elements. Hence optimization of the adder both in terms of speed and/or power consumption must be pursued. During the design of an 1 bit full adder we have to make two choices for different design abstraction levels. One is accountable for the adder's architecture implemented with the one-bit full adder as a building block. The other defines the particular design style at transistor level to implement the one-bit full adder. The one-bit full adder used is a three-input two-output block. The inputs are the two bits to be added, A and, B and the carry bit C_i, which is the calculations of the previous digits. The outputs are the result of the sum operation S and the result of the of the carry bit operation C_o. More specifically, the sum and carry output are given by

$$S = A \oplus B \oplus Ci = A\overline{BCi} + \bar{A}B\bar{C}\imath + \overline{AB}Ci \ldots\ldots 1$$
$$Co = AB + (A + B)Ci \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots .2$$

From equation (2) it is evident that if A=B the carry output is equal to their value $C_o = C_i$ and the full adder has to wait for the computation of C_o. Until now, in the literature there have been some comparisons between full adder circuits. However, in the former work, no low-power topologies were realized at all, whereas in the latter, new topologies which appear to be promising is not taken into account. Moreover, the effects of the interconnection parasitic of low-power full adders in were extracted from layout only for the CMOS and CPL topologies, whereas they were only roughly estimated for the other circuits. For these reasons, these estimated results differ from those presented in this paper. Apart from and, no systematic comparisons have been developed in the literature for other topologies, and newly proposed circuits are compared to existing ones by applying different simulation and comparison strategies, and by using different technologies. Hence, it is not simple to compare performances in a fair and clearly understandable manner. The analysis and comparison developed here have been carried out in terms of speed, power consumption and delay product. The investigation, which also includes the most interesting recently proposed one-bit full adders, has been based on simulation runs on a Cadence environment by using a 0.45nm process taking parasitic into account, since post layout simulations have been performed. Two different design strategies have been used to size each topology. The former one is used to minimize power consumption adopting minimum-size transistors, the latter one is minimum power-delay product by suitable

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transistor sizing. Performance for both plan strategies has been also compared for different supply voltage values.

II The 10T Adder

The circuit of 10T Adder is a one-bit full adder core has three inputs (A, B, and carry in Ci) and two outputs (sum S and carry out Co). The Adder cell is made of five CMOS inverters that are connected as shown in fig1. Input A is directly connected to inverter first while input B is connected second and third inverter. Second inverter PMOS drain and third inverter NMOS drain are connected first inverter output while second inverter NMOS drain and third inverter drain are connected directly input A. Second inverter output is connected fourth inverter input and input Ci is given in inverter fifth. There is interesting, the power supply V_{DD} connected first inverter only. All transistors have minimum length (L_{MIN} =45nm according to used Technology), while their widths are typically design parameters. The value of W_{N1} and W_{N2} defines the NMOS driver transistors width use in first inverter CMOS Invertors and the value of W_{P1} and W_{P2} defines PMOS transistors width.

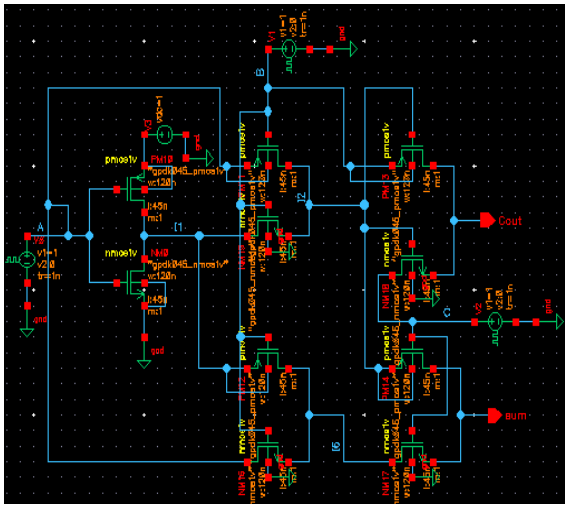

Fig-1 Ten Transistor Adder cell

Based on CMOS 0.45-nm process technology, the proposed full adder is proven to have the minimum power consumption and less power-delay product by Cadence simulation comparing with other prior literature, the characteristics of the novel hybrid full adder shows that the design has the best power-delay product for carry out signal. Due to the minimum time delay of carry out, the adder core greatly improves the overall performance for a large scale of multi-bit adder. In active mode of operation the high Vt transistors are turned off and the logic gates consisting of low Vt transistors can operate with low switching power dissipation and smaller switching time. In standby mode, the high Vt transistors are turned off thereby cutting off the internal low Vt circuitry.

III Low power 1-bit full adder

Most often, Full adder is a part of the critical path that determines the overall performance of a system. 1-bit full adder is one of the most significant components of a processor that determines its throughput. In this paper I have designed a new 1-bit 10-transistor full adder which dissipate less power than the standard implementations of full adder cell. The proposed adder is tested and compared with the high transistor count and existing 10-transistor adders under the same conditions. The addition of 2 bits A and B with C yields a SUM and a CARRY bit. The integer equivalent of this relation is shown as

….3

…….…..... 4

The proposed adder implements equations (3) and (4) using complementary CMOS and MUX based design logic with only 10 transistors. The adder is useful in larger circuits such as multipliers despite the threshold problem. The number of direct connections from VDD to the ground is reduced in the new design to minimize the power consumption due to short circuit current. Also the generation of SUM from CARRY is avoided as in the CMOS adder. Performance analysis of all the adder designs is carried out in 180nm, 90nm and 45nm CMOS technology in cadence. The performance is studied at power supply voltage of1.8V for 180nm, 1.0V for 90nm and 0.7V for 45nm at frequencies of 50MHZ.

IV CMOS Inverter Leakage Current

Dynamic power dissipation appears only when a CMOS gate changes from one stable state to another stable state. Thus, the power consumption can be reduced if the switching activity of a given logic circuit is reduced without changing its function. A straight approach is to design a full adder (FA) that consumes less power. In the CMOS devices, the leakage current is becoming a major contributor to the total power consumption. Therefore Low threshold voltages, sub threshold and gate leakage in current deep-sub micron technology have become main sources of leakage and are expected to increase with the technology scaling. The leakage power is becoming significant component of the total power and may contribute to majority of the power dissipation in future *CMOS* technologies. The leakage current and leakage power are increasing with scaling. Dynamic power dissipation and static power dissipation are the two main sources for power dissipation in CMOS circuits. Static power dissipation

occurs due to leakage current when the transistor is usually off.

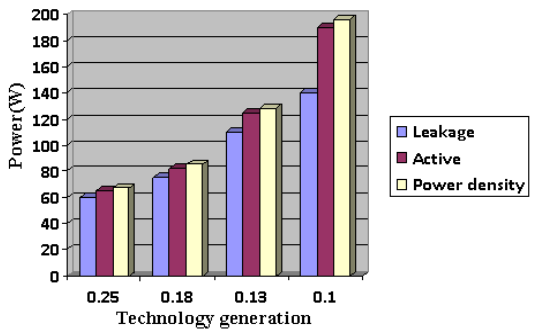

Fig-2. Static and dynamic power trends

The improvement in technology scaling has introduced very large sub threshold leakage current, hence careful design techniques are very important in order to reduce sub threshold leakage current for low power design .Leakage current emerge in both active and standby modes. It is suggested to switch off the leakage current when the circuit is in standby form. Technology graphs and power are shown in fig-2.

There are two major leakages current for power wastage in CMOS inverter

1. Sub threshold (weak inversion) leakage (I_{SUB})
2. Oxide tunneling Current (I_G)

Where sub threshold leakage current are explain in mathematical as

$$I_{SUB} = \frac{W}{L}\,\mu V_{th}^{2} C_{STH}\, e^{\frac{Vgs-Vt+\eta Vds}{n\,Vth}}\left(1-e^{\frac{-Vds}{Vth}}\right) \quad ..5$$

where W and L denote the transistor width and length, μ represents the carrier mobility, $V_{TH} = \frac{kt}{q}$ is the thermal voltage at temperature T , $C_{STH} = C_{DEP} + Cit$ denotes the summation of the depletion region capacitance and the interface trap capacitance both per unit area of the MOS gate and ɳ is the drain-induced barrier lowering (DIBL) coefficient is the slope shape factor and is calculated by equation-2

$$n = 1 + \frac{Csth}{Cox} \quad \ldots\ldots\ldots\ldots \quad 6$$

Hence the Oxide tunneling Current (I_G or I_{FN}) explain as

$$J_{FN} = \frac{q^3 E^2 ox}{16\pi^2 h \emptyset ox} e^{-\frac{\emptyset^{3/2} ox\, 4\sqrt{2m}}{3hqEox}} \quad \ldots\ldots\ldots..7$$

Where E_{OX} is the field across the oxide; $Ø_{OX}$ is the barrier height for electrons in the conduction band; and m^* is the effective mass of an electron in the conduction band of silicon. The FN is the current equation which represents the tunneling through the triangular potential barrier and is legal for $V_{OX} > Ø_{OX}$, where is the voltage drop across the oxide

V Leakage Reductions at Process Level

In a full adder, the total power dissipation in dynamic and static components during the active mode. In the standby mode, the power dissipation is due to the standby leakage current. There are two major sources for Dynamic power dissipation. First is the switching power due to discharging and charging of load capacitance. The second is short circuit power occurs due to the nonzero rise and fall time of input waveforms. The static power of a CMOS circuit is calculated by the leakage current through each transistor. The dynamic (switching) power (P_D) and leakage power (P_{LEAK}) are expressed as

$$P_D = \alpha f C V_{DD}^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots 8$$
$$P_{LEAK} = I_{LEAK}.\, V_{DD} \quad \ldots\ldots\ldots\ldots\ldots\ldots 9$$

Where α is the switching activity; f is the operation frequency; C is the load capacitance. The substrate doping concentration should be proportionally increase to decrease the depletion width. The theory of constant field scaling lies in scaling the device voltages and the device dimensions by the same factor, In addition to gate oxide thickness and junction scaling, another technique is used to improve short-channel characteristics is fine engineering. By changing the doping profile in the channel region, the distribution of the electric field can be changed. The purpose is to optimize the channel profile to minimize the OFF-state leakage while maximizing the linear and saturated drive currents.

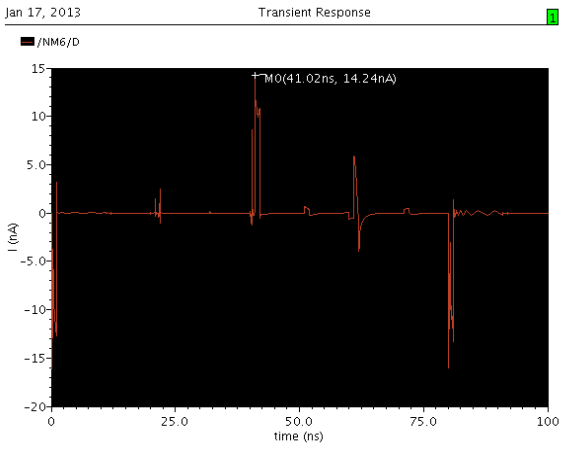

Fig-3(a) Leakage current of Adder

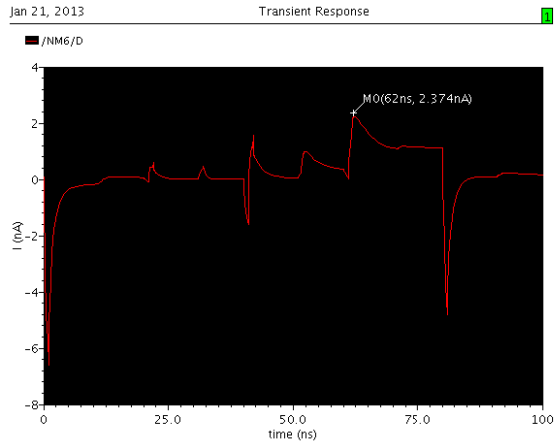

Fig-3(b) Leakage current after improve on process level

VI Leakage Reductions at Circuit Level

At the circuit level we can reduced leakage by some technique they self reverse biasing, multiple threshold voltage, gated Vdd/Ground.

a) Self Reverse Biasing

The body effect in CMOS transistors, a smaller width of the depletion layer leads to lower V_T. The reverse biasing of CMOS transistor increases V_T while on forward biasing of the COMS transistor V_T decreases. And also in CMOS threshold voltage increases with increased doping of the channel but decreases with applied bias. Therefore the current in the sub threshold region can be partially decreased by reverse biasing. Equation (10) quantifies the back-gate bias parameter as function of the oxide capacitance and substrate doping level.

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_____ .. . … … … … . . . 10

Where is gate oxide thickness, is substrate doping level q is unity electron charge is gate oxide permittivity and is Silicon permittivity.

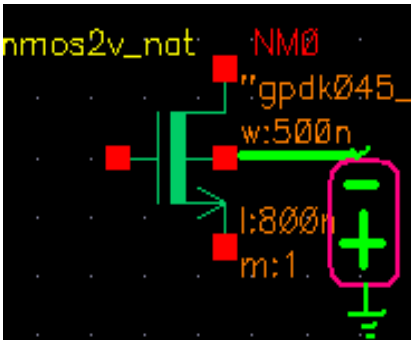

Fig 4(a) MOS Transistor with reversed bias

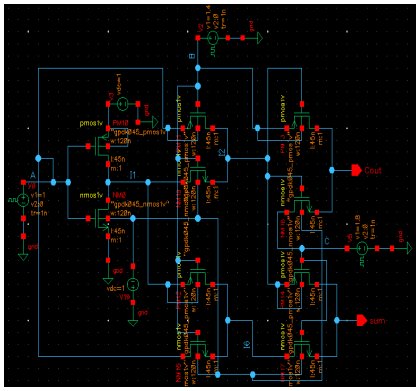

Fig 4(b) 10T Adder circuit with reverse bias

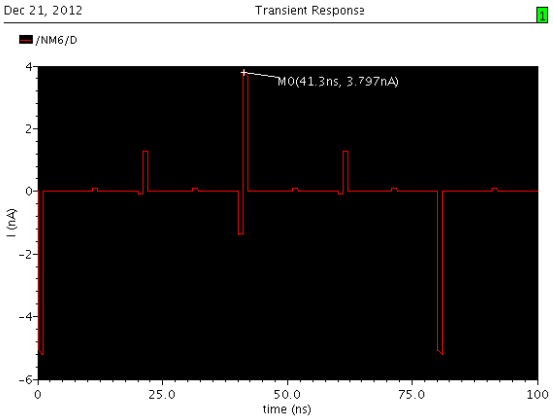

Fig5 (a) Leakage current without reverse bias

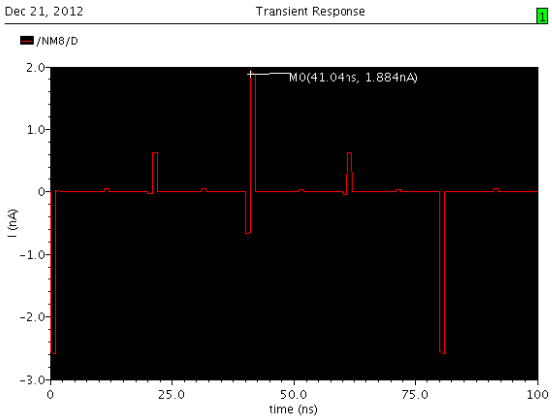

Fig 5(b) Leakage current with reverse bias

b) Multiple channel doping

The threshold voltage is equals to the summation of the flat band voltage, twice the bulk potential and the voltage across the oxide due to the depletion layer charge.

$$V_T = V_{FB} + 2\varphi_F + \frac{\sqrt{2 \in_q qN_a(2\varphi_F + V_{SB}}}{C_{OX}}$$

Where the flat band voltage, V_{FB} is given by

$$V_{FB} = \varphi_{FB} - \frac{Q_F}{C_{OX}} - \frac{1}{C_{OX}} \int_0^{t_{OX}} \frac{x}{x_{OX}} \rho_{OX}(x)dx$$

With

$$\varphi_{MS} = \varphi_M - \varphi_S = \varphi_M - (x + \frac{E_g}{2q} + \varphi_F)$$

And

$$\varphi_F = V_t \ln \frac{N_a}{n_i}, p - substrate$$

And the similar for pMOS

$$\varphi_F = V_t \ln \frac{N_d}{n_i}, n - substrate$$

The threshold voltage dependence on the doping density is illustrated with for both *n*-type and *p*-type MOSFETs with an aluminum gate metal.

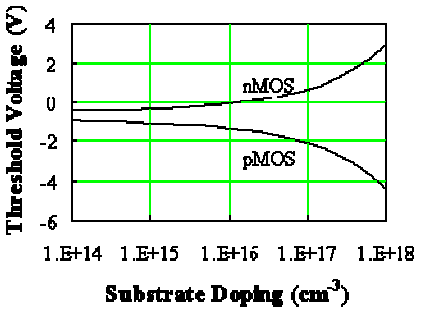

Fig-6 Threshold voltage of *n*-type (upper curve) and *p*-type (lower curve) MOSFETs versus substrate doping density

The threshold of both types of devices is slightly negative at low doping densities and differs by 4 times the absolute value of the bulk potential. The threshold of nMOS increases with doping while the threshold of pMOS decreases with doping in the same way.

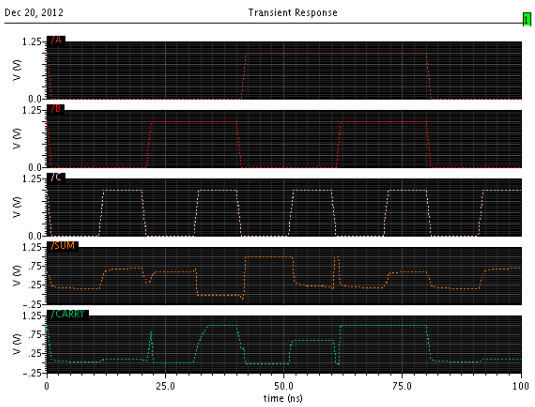

Fig-7 Transient Response with multiple doping

VII Simulation and Result

We simulate various Adder cell on cadence tool in different-different technique and circuit parameter in 10T Adder and other and found that 10T Adder is the most prominent low power consumption cell. The leakage power is reduced by high level using various techniques. We have clear that V_T is the most appropriate parameter for reducing leakage power and leakage current. By increasing doping and decreasing T_{OX} reduced power consumption. The Equation-11 show that the threshold voltage dependent on various parameters on Adder cell. Here we can see that the threshold can changed by Ø, γ and η. They are easily change by well engineering design.

$$V_T = V_{TO} + \gamma(\sqrt{(-2\emptyset f) - V_{SB}} - \sqrt{2\emptyset} \ldots\ldots 11$$

A variation of the flat band voltage cause due to oxide charge will cause a reduction of both threshold voltages if the charge is positive and an increase if the charge is negative.

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