Static and Transient Stability Enhancement of Power System by Optimally Placing UPFC(Unified Power Flow Controller)

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***Abstract*— Proper placement of FACTS devices is very important for the rapid and successful operation because of high cost and circuit complexities. In this paper best location of UPFC (Unified Power Flow Controller) is obtained both for static and transient voltage stability enhancement of an IEEE 14 bus power system. The simulation is done on PSAT (Power System Analysis Tool-box) in MATLAB and optimal location is found out by Continuation Power Flow (CPF) and Line stability index. The bus having lowest voltage is the critical bus and the line having largest value of index for maximum permissible load with respect to a bus is the most critical line referred to that bus. It is found that by properly placing UPFC loadability margin of the system has been increased considerably leading to improvement of voltage stability and stability index value decreases at each reactive load with the insertion of the device at right place. Transient stability analysis is also done for an IEEE 14 bus system with a fault created at a bus. It is found from the time domain simulation that proper placement of UPFC increases the transient performance of the system by damping out the power oscillation under large disturbance conditions.**

Keywords—**UPFC, FACTS, CPF, index, stability**

I. INTRODUCTION

The power system should be operated so that voltage and power should be within acceptable range. Control of active and reactive power flow is very important for the operation of power system. Reactive power imbalance causes voltage instability of the system. Real and reactive losses become very high when the system is operating at peak load. The system in this situation can be made stable by reducing the reactive load or by providing a source of reactive power at the right place before voltage collapse. In case of a disturbance or a fault the basic requirement is to make the synchronous generators to run in synchronism after a disturbance occur in the system. Whenever a perturbation is there in the system the generators tend to lose synchronism and if they re-maintain to run at the same speed the system. If the oscillations after disturbance are damped and the system comes to new operating point it is said to be stable. If the oscillations after a disturbances are damped and the system comes to new stable operating point hence it is called stable. Due to increased operations which results in making the power system to be highly stressed, the need for dynamic stability is arising. Transient stability assessment is a part of dynamic security assessment of power system which determines the ability of the system to remain in equilibrium when subjected to disturbances.

The revolution of Power Electronics Technology has given opportunities for developing the FACTS devices for stable operation of power system. In the last two decades number of Power Electronic based devices are implemented and known as FACTS (Flexible AC transmission System).These devices are effectively used for voltage control, power flow control, harmonic elimination, damping oscillation and improving transient stability and minimization of losses[10],[12]. Many FACTS devices are widely used like SVC (Static Var Compensator), STATCOM (Static synchronous Compensators), UPFC, TCSC. All these FACTS devices have their own advantages to control active and reactive power for static and dynamic voltage stability. Also whenever a disturbance occurs in the system like load imbalance or any fault, the system loses stability and the generators go out of synchronism. Proper placement of FACTS devices help in improving the transient stability [1] [8]. To achieve good performance of these devices optimal placement is very important as the cost of these devices is very high. Calculation of Stability indices is very effective method o find out the critical bus a and line of the system. Using power flow these indices can be calculated and the line having maximum value of the index is the most critical line referred to the bus. [7] Various techniques have been implemented in previous research papers to find out the location of these devices using stability indices but they involve numerous complexities in power flow solution and calculations of indices. [11], [13]

In this paper simple and effective method has been implemented for finding the best location of FACTS device based on static and transient stability using Continuation Power Flow (CPF), stability index and time domain simulation. Simulations are carried out in PSAT software which is very user friendly. Critical bus is determined using P-V curve and the Critical line is determined using the Line stability index. The line having maximum value of the index in the most critical line corresponding to that bus. The selection of best possible location of UPFC is carried out both for steady state and transient stability enhancement of a IEEE 14 bus system and it is found that proper placement of UPFC gives the static and transient stability improvement of the power system.

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II. STUDY SYSTEM

The IEEE 14 bus system modeled in PSAT software is shown in fig 1

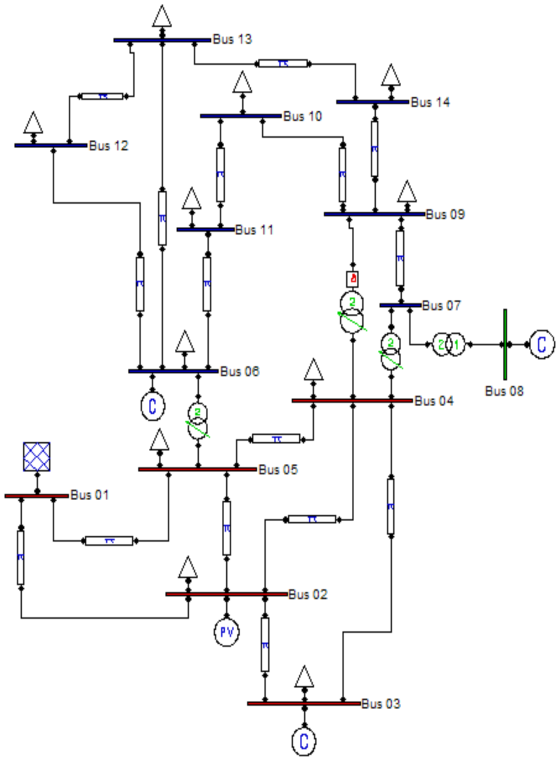

Fig 1 IEEE 14 bus system

III. METHODOLOGY

A. *Continuation Power Flow*

The graph is obtained between the bus voltage and the loading factor λ by Continuation Power Flow is known as P-V curve. It determines the loadability margin i.e. the margin between the voltage collapse point and current operating point.

B. *Line Stability Index*

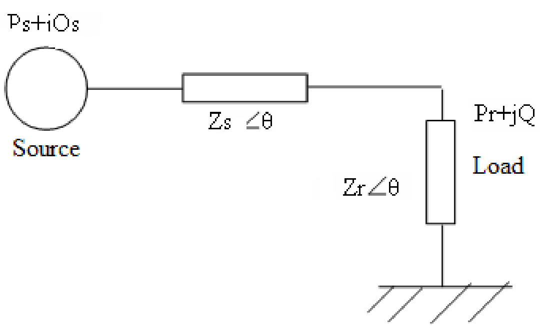

Fig 2 shows a network having a generator, transmission line and load.

$Z_s \angle \theta$ =line impedance

$Z_r \angle \varphi$ =load impedance

$\tan \phi = Q_r / P_r$

With the increase in load, current decreases. This leads to voltage drop at the receiving end

$$I = \frac{V_s}{\sqrt{[(Zs\cos\theta + Zr\cos\phi)^2 + (Zs\sin\theta + Zr\sin\phi)^2]}} \quad (1)$$

$$V_r = Z_r I Z_r / Z_s \frac{V_s}{\sqrt{[1+(Z_r/Z_s)^2 + 2(Z_r/Z_s)\cos(\theta-\phi)]}} \quad (2)$$

Power at the receiving end

$$P_r = V_r I \cos\varphi \quad (3)$$

and

$$Q_r = V_r I \sin\varphi \quad (4)$$

Line Stability Index L is

$$L = 4[Vi^2(P_{(i+1)}r_i + Q_{(i+1)}x_i) + (P_{(I+1)}\, x_i + Q_{(i+1)}r_i)^2]/V_i^4 \quad (5)$$

The value of index should be less than 1 for a stable system.

IV. SIMULATION RESULTS

A. *Static Voltage Stability*

P-V curve

The variation of bus voltage with the loading factor λ is obtained for IEEE 14 bus system. Continuation Power Flow has been done in PSAT software and it is found that bus no 14 is the most insecure bus as the voltage at each reactive load of bus 14 is minimum. The figure 3 shows the P-V curve for the lowest three voltage buses without UPFC Fig 4 shows the P-V curve for three lowest voltage buses with UPFC between 9-14. It is clear that the loadability margin has been increased considerably to 50 % with the insertion of UPFC in the system results in the increase in system stability.

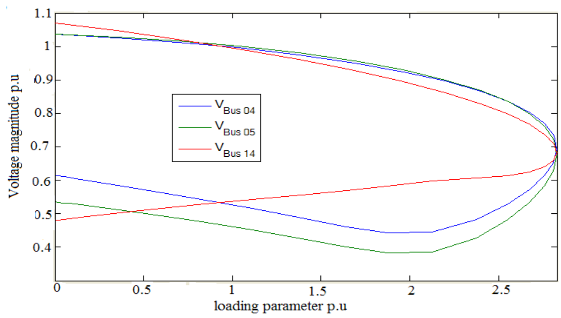

Fig 3 Lowest three bus voltages without FACTS

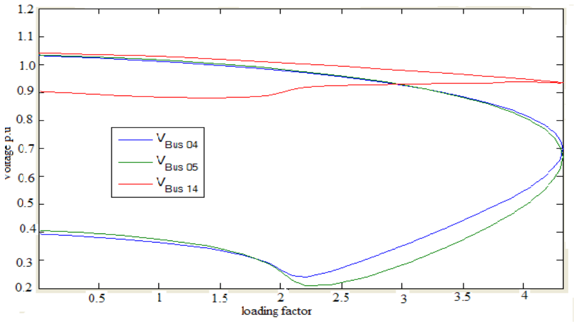

Fig 4 Voltages with UPFC

Dtermination of most crtical lines

Step 1: Reactive load at a bus is gradually increased keeping all other loads constant.
Step 2: Load flow is done using PSAT to find out the active and reactive power transmitted at the receiving end for a particular load.
Step 3: Maximum Active and reactive power that can be transferred to a particular bus is calculated using the given formula.
Step 4: Stability index is calculated at each load knowing power transmitted using load flow.
Step5: This is repeated for each bus and index is calculated for each line associated with bus.
Step 6: The line having maximum value of the stability index at maximum loadability point is the most critical line with respect to that bus.

Table 1 shows the stability index for most stressed lines without UPFC and the results show that the line 13-14 is the most critical line with respect to bus 14 and Table 2 shows the same with UPFC at different locations. It is clear from the table that insertion of UPFC between line 9 -14 reduces the index for each line considerably increasing the loadability margin of each bus.

TABLE 1 STABLITY INDICES WITHOUT UPFC

Load p.u	Line No	Line stability index
Q_{14}=0.9	13-14 9-14	0.869 0.746
Q_{10}=0.948	11-10 9-10	0.363 0.241
Q_{12}=0.855	6-12 13-12	0.598 0.379

TABLE 2 STABLITY INDICES WITH UPFC

Load p.u	Line No	Line Stability index		
		UPFC (9-14)	UPFC (9-10)	UPFC (12-13)
Q_{14}=0.9	13-14	0.654	0.864	0.791
Q_{10}=0.948	11-10	0.352	0.404	0.372
Q_{12}=0.855	6-12	0.593	0.595	0.591

Fig 5 shows the variation of stability index for three stressed lines without UPFC and fig.6 shows the index with the device. It is clear that from the figure the value of index decreases at each reactive load when the device is placed optimally between 9& 14 increasing the system stability. With the insertion of UPFC at the right location increase the maximum load handling capability of each bus.

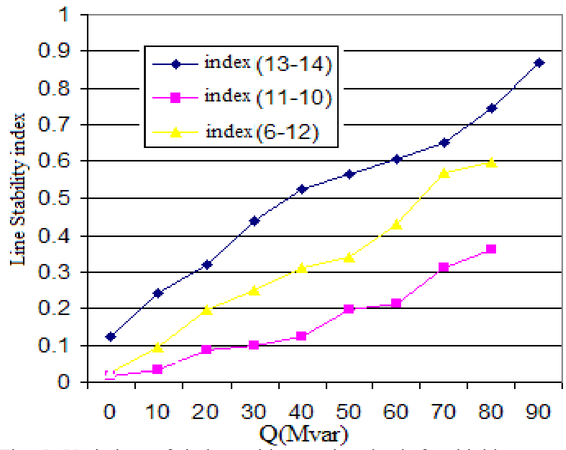

Fig 5 Variation of index with reactive load for highly stressed lines without FACTS controller

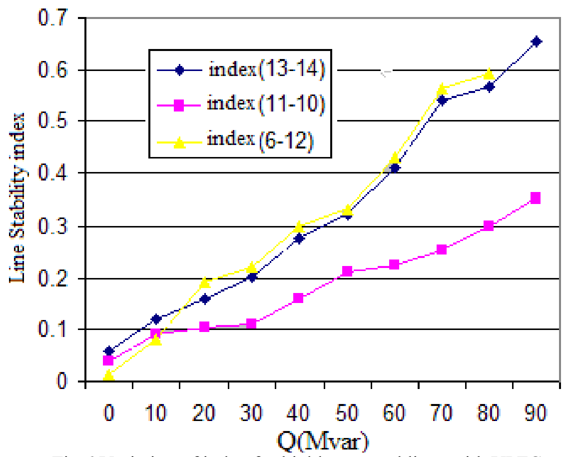

Fig 6 Variation of index for highly stressed lines with UPFC

B. Transient Stability

Time Domain Simulation

A three phase to ground fault is created at bus 5 and time domain simulation is done using PSAT software the eigenvalue plot is obtained and the eigenvalues for the different states are obtained without UPFC. Figure shows the graphs of relative rotor angles, angular velocities and voltage profile of IEEE 14 bus system without UPFC. A three phase fault is created at bus 5 at 1 sec and cleared at 1.2 sec. The figs 7(a)-(e) shows the graphs of relative angles, angular speeds and voltages. It is clear from the results that after the fault is cleared the settling time are more with oscillations leading to system instability

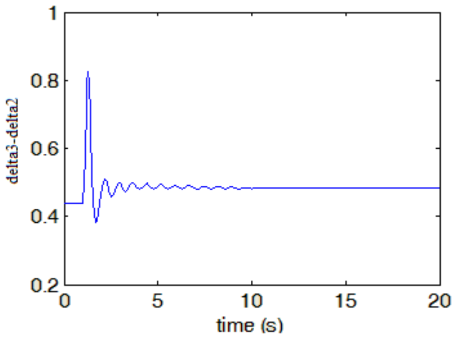

Fig 7(a) Relative rotor angle32

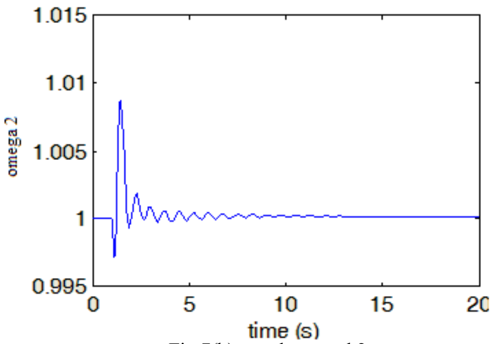

Fig 7(b) angular speed 2

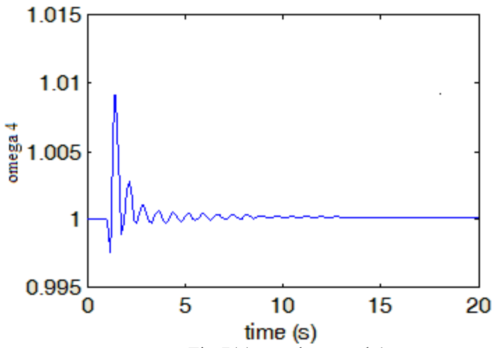

Fig 7(c) angular speed 4

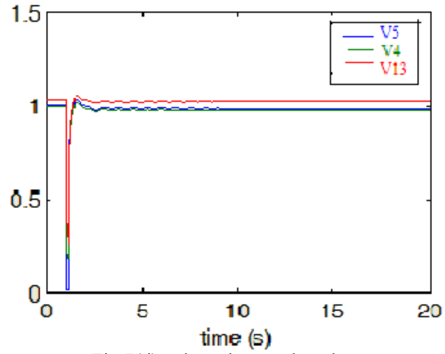

Fig 7(d) voltage lowest three buses

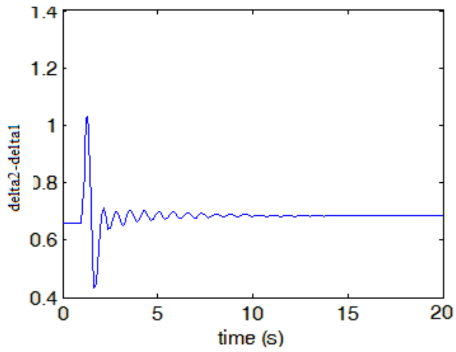

Fig 7(e) Relative angle 21

UPFC is placed at various locations near to the bus where fault is there and the time domain simulation is done for each location. It is found that when UPFC is placed between line 1&5 the system reaches to steady state rapidly and the oscillations die out in very less time as compared to when the device was not connected. It is clear from the voltage graphs that transients in the voltages of the buses die out rapidly with the insertion of UPFC at proper location. Fig 8(a)-(g) shows various graphs of relative angular positions, angular velocities of individual generators and voltages. It is clear from the results that with the insertion of UPFC at the proper location transient behavior is improved. So when fault is located at bus 5, the best location of UPFC is between lines 1-5.

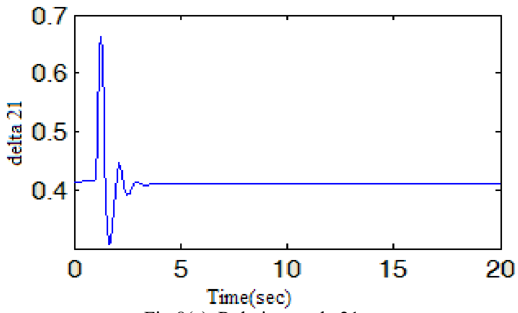

Fig 8(a) Relative angle 21

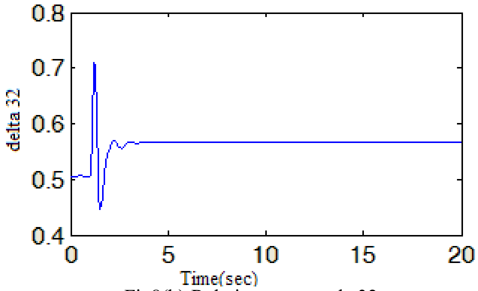

Fig8(b) Relative rotor angle 32

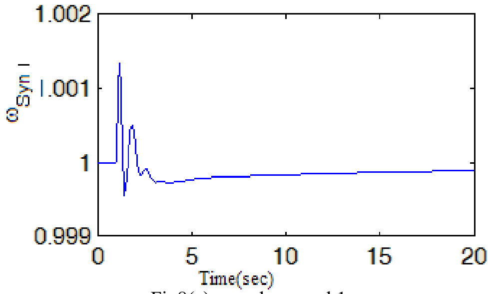

Fig8(c) angular speed 1

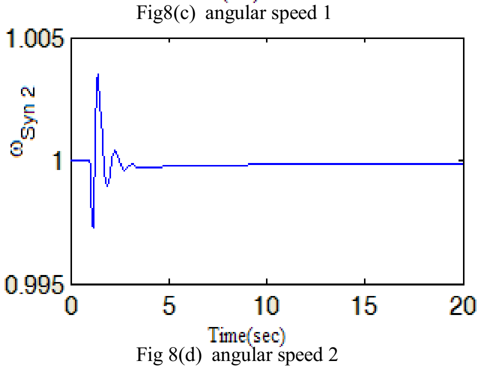

Fig 8(d) angular speed 2

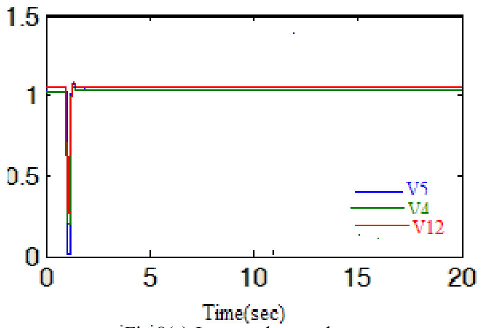

Fig 8(e) Lowest three voltages

V. Conclusion

Static and Transient stability enhancement of IEEE 14 bus system is done with the help of UPFC. Simulation is carried out in PSAT software and critical line and weakest bus is determined using CPF and stability index. Proper placement of UPFC enhances the steady state and transient stability of the system. Fault is created at a bus and the results show that by properly placing UPFC, settling time of the system can be reduced considerably making the system stable with fewer oscillations.

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