Test Input Vectors for Supply Current Testing of TTL Combinational Circuits

Masaki Hashizume Takeomi Tamesada Isao Tsukimoto

Faculty of Engineering, The University of Tokushima

Tokushima-shi Tokushima 770 JAPAN

Abstract

In this paper, test input vectors for ISCAS-85 benchmark circuits are derived, with which single faults of each signal line in the TTL combinational circuits can be detected by their quiescent supply currents. Also, they are compared with the vectors for fault detection methods based on the primary output logic values. It is shown that by detecting faults with supply currents of TTL circuits, smaller size of test inputs can be derived for most of the circuits than fault detection methods based on the primary output logic values, and also, if both the output logic values and the supply current are used for detecting faults, the number of the test inputs can be reduced.

1. Introduction

Until now, it is shown that supply current testings, especially the IDDQ testing for CMOS circuits, are very useful for realizing high reliable systems[1,2,3]. In order to detect faults, the IDDQ testing utilizes the property that if any defects do not occur in CMOS circuits, the extremely less supply current has appeared.

The IDDQ testing has a good property to make it easy to generate test vectors, which is called as "automatic observability"[4]. That is, in the process of the IDDQ testing, faults must be sensitized, like in fault detection methods based on primary output logic values, but the effects of the faults do not have to be always propagated to any primary outputs, because faults can be detected by the IDDQ testing if any effects of faults are generated in the supply current. By using this property to detect single stuck-at faults in CMOS circuits, a fault simulation algorithm can be simplified, the size of test vectors can be reduced and the fault coverage can be increased[3]. Also, it is reported that the IDDQ testing can detect some of redundant faults, which can not be detected by measuring the output logic values[5]. Furthermore, the usefulness of the current testing has been checked for single stuck-at faults in CMOS circuits[6].

However, the effectiveness of the supply current testing for TTL circuits is not shown. Besides CMOS circuits, TTL circuits, in which TTL gates are used, are well used now for implementing logical systems. For TTL circuits, quiescent supply currents flow from the Vcc terminal to the GND terminal, even if any faults do not occur in the circuits. Thus, the IDDQ testing methodology is not applicable to fault detection problems of TTL circuits.

In order to detect faults in TTL circuits with their supply currents, a new fault detection method for TTL circuits should be developed. Therefore, we proposed fault detection methods based on supply currents of TTL circuits[7,8]. In order to detect faults, the methods utilize each test vector and the supply current which flows through the Vcc terminal when the test vector is inputted to the unfaulty circuit, instead of the output logic values. On testing circuits, after each test vector is inputted, the quiescent supply current is measured and it is checked whether the current is almost the same as the unfaulty circuit. If the measured supply current is different from the unfaulty circuit, the circuit is determined as a faulty circuit. Since it needs a lot of memory to store the supply current of the unfaulty circuit, the method in [8] uses the maximum, the minimum and the average values, and the linear predictive coefficients as characteristic parameters of

0-8186-2985-1/92 $03.00 © 1992 IEEE

the supply current, and detects faults with a pattern recognition technique.

In [8], the effectiveness is checked by some experiments. However, the test input vectors and the fault coverage have not been shown. Therefore, in this paper, the reduced test vectors and the fault coverage of the supply current testing for TTL circuits are presented.

Many faults can be detected by measuring the output logic values, even if the test input vectors for the current testing are used. Therefore, it seems that if both the supply current and the primary output logic values are measured for detecting faults, the size of test vectors and the CPU time can be decreased. In this paper, the effectiveness obtained by measuring both the supply current and the output logic values is examined.

In section 2, our supply current testing method is described. In section 3, a test generation algorithm and the evaluation results are presented.

2. Supply current testing for TTL circuits

2.1 Principle of fault detection

Fig.1 shows examples of supply currents of a 2 bit full-adder circuit, which is made of TTL LS-type ICs. As shown in Fig.1(a), the supply current of the unfaulty TTL circuit changes with each test inputs.

If a fault occurs in the circuit, a different supply current is generated as shown in Fig.1(b). We attempt to detect faults with the difference of quiescent supply current between the CUT and the unfaulty circuit,

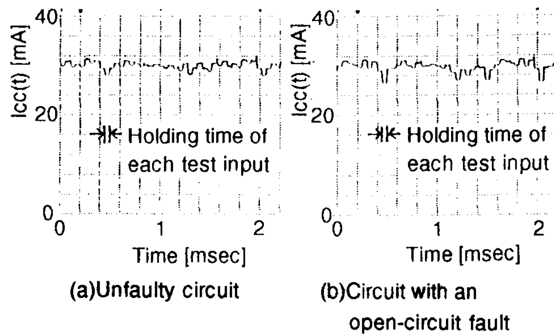


Fig.1 Examples of supply current of TTL circuits. (Sampling frequency=125kHz)

because dynamic currents are difficult to be measured.

The supply current(Icc(j)) of a TTL circuit can be provided by (1).

$$Icc(j)=\sum_{i=1}^{N} Ii(j) \quad (1)$$

where N is the number of gates in the circuit, and Icc(j) and Ii(j) are supply currents of the CUT and the i-th gate, respectively, which will flow when the j-th test vector is inputted to the primary input terminal of the circuit. Supply currents of TTL gates depend on the output logic values[7,8]. Therefore, if a fault occurs in a CUT, and the different output logic values from the unfaulty circuit are generated, Icc(j)' in (2) will be appeared, which is different from the unfaulty circuit.

$$Icc(j)'=\sum_{i=1}^{N} Ii(j)' \quad (2)$$

where Ii(j)' is the supply current of the i-th gate in the faulty circuit.

By using the difference of supply current between the unfaulty circuit and the CUT, it is expected that faults in TTL circuits can be detected. Therefore, in the method proposed here, faults are detected by ΔIcc(j), which is defined by (3).

$$\Delta Icc(j)=|Icc(j)-Icc(j)'| \quad (3)$$

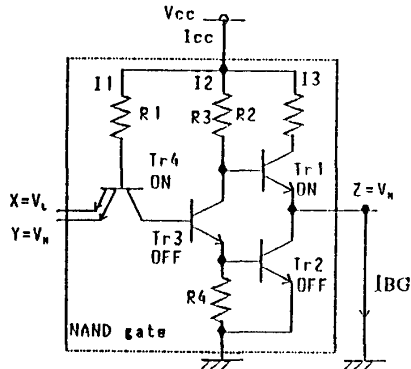
2.2 Faults in TTL circuits

There are many kinds of faults that can occur in TTL circuits. However, in this paper, only faults of each signal line are considered. For TTL circuits implemented on printed boards, the faults are realistic. That is why any faults will not occur in ICs used in printed boards since each IC has been well checked before shipping, but more faults will occur at signal lines since the width of printed patterns has become more narrow. For the circuits implemented in ICs, many faults occur at signal lines[9]. Therefore we attempt to detect faults of signal line in this paper.

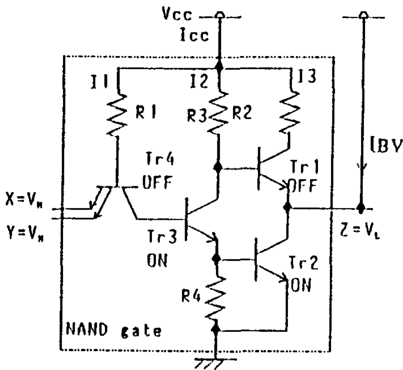
As faults to be detected of each signal line, we consider only an open-circuit fault and bridge faults with either the Vcc lines or the GND lines, because physical faults occur well at signal lines as described above and both the Vcc lines and the GND lines occupy the large area in implemented logic circuits.

If an open-circuit fault occurs at an output signal

line of a gate, the logic value of the line is 1(High voltage), and there are no effects on the supply current. Therefore, if and only if output logic values of any gates between the faulty signal line and primary output signal lines are changed by the fault, it can be detected by our method. If a bridge fault with the Vcc(GND) lines occurs, the effect can be modeled as a stuck-at-1(0) fault. Furthermore, a large amount of current will flow at the signal line, when the fault is sensitized, as in Fig.2.



(a)Bridge fault with GND line



(b)Bridge fault with Vcc line

Fig.2 Supply currents of TTL NAND gate with bridge faults.

Table 1 shows examples of the supply currents of each gate. The supply currents of unfaulty gates in Table 1 are obtained by dividing the supply currents of the ICs by the number of gates implemented in them. The supply currents of faulty gates are obtained by subtracting the currents of unfaulty gates in Table 1 from the supply currents of the faulty ICs. As shown in Table 1, supply currents of faulty gates are specified with the minimum and the maximum values, since they change with time and with different ICs.

Table 1 Examples of supply currents of TTL gates.

Logical function	NI	I_L [mA]	I_H [mA]	I_{BG} [mA]	I_{BV} [mA]
NOT	1	0.71	0.23	74.80~82.80	108.50~132.50
BUFFER	1	0.81	0.47	82.05~85.60	157.00~206.00
AND	2	1.10	0.56	45.85~53.00	73.20~ 78.50
AND	3	1.17	0.59	47.10~60.40	57.35~ 63.65
NAND	2	0.70	0.18	40.30~49.20	156.00~207.60
NAND	3	0.73	0.20	51.10~56.40	100.00~268.00
OR	2	1.32	0.73	46.20~52.20	82.60~ 88.05
NOR	2	1.03	0.50	38.00~44.50	118.00~238.00
NOR	3	1.16	0.72	31.35~37.25	94.00~188.00
EX-OR	2	1.57	0.96	72.20~77.20	50.00~ 53.80

NI is the number of inputs.
I_L (I_H) is the supply current of the unfaulty gate, whose output logic value is 0(1).

2.3 Supply current measurement

There are many methods to measure supply currents. In this paper, the method in Fig.3 is used; i.e. supply currents are measured by amplifying the voltage across a resistor R, which is inserted between the Vcc terminal of the CUT and the source voltage terminal.

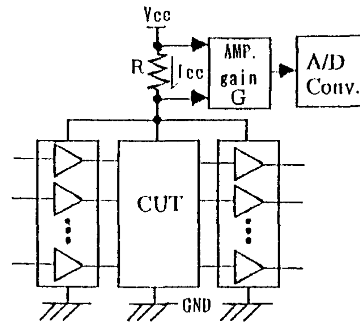


Fig.3 Supply current measurement circuit.

There are some constraints, which must be satisfied in order to measure supply currents correctly by the method. The analog input voltage to an A/D converter

should be less than its analog maximum quantization size(Vadmax). Also, in order for TTL gates to work, the supply voltage should be within the specified range(from Vccmin to Vccmax); for example, for the 74 LS type of TTL gates, Vccmin=4.75[V] and Vccmax=5.25[V]. Therefore, (4) and (5) should be satisfied.

$$G \cdot R \cdot Icc(j) \leq Vadmax \quad (4)$$

$$Vccmin \leq Vcc - R \cdot Icc(j) \leq Vccmax \quad (5)$$

A CUT, whose supply current does not satisfy either (4) or (5), can be determined easily as a faulty circuit, if the supply current of the unfaulty circuit satisfies both (4) and (5). Therefore, R and G are determined so that the supply current of the unfaulty circuit can satisfy both (4) and (5).

Since if a fault bridging with the GND line is occurred and sensitized, a large amount of current flows at the faulty line in many cases, it can be detected easily. But even if a primary input signal line is bridging with the GND lines, the faulty current does not flow through the Vcc terminal of CUT. Therefore, in order to make it easy to detect such faults, a gate is inserted at each primary input terminal. Also a gate is inserted at each primary output terminal in order to detect the open-circuit fault, because if the gates are not inserted, when an open-circuit fault occurs at a primary output signal line, the effect of the fault does not appear in the supply current.

All faults in the gates inserted at the primary input and output signal lines can be removed easily by testing them fully, since they are the most primitive gates. Thus we assume that the inserted gates have no fault.

2.4 Test vectors for current testing of TTL circuits

The testing method proposed here is based on $\Delta Icc(j)$, that is, it is determined by (3) whether a circuit is faulty. However, faults should be detected by (6), since there is a constraint on the resolution(Idiv) for measuring supply currents, which is defined by (7).

$$\Delta Icc(j) \geq Idiv \quad (6)$$

$$Idiv = \{Vadmax/(2^k-1)\}/(G \cdot R) \quad (7)$$

where a k bits A/D converter is assumed to be used.

Also, the supply current of faulty gate(Ik(j)') is defined by (8) from Table 1.

$$Ifmin(j) \leq Ik(j)' \leq Ifmax(j) \quad (8)$$

Therefore, by using (9) and (10), it can be determined whether an input vector(Tj) can be used as a test input.

$$|max(Icc(j)')-Icc(j)| \geq Idiv \quad (9)$$

$$|min(Icc(j)')-Icc(j)| \geq Idiv \quad (10)$$

where

$$max(Icc(j)') = \sum_{i=1}^{k-1} Ii(j) + Ifmax(j) + \sum_{i=k+1}^{N} Ii(j) \quad (11)$$

$$min(Icc(j)') = \sum_{i=1}^{k-1} Ii(j) + Ifmin(j) + \sum_{i=k+1}^{N} Ii(j) \quad (12)$$

Furthermore, since (13) is always satisfied, we select an input vector, which can satisfy either (14) or (15), as a test input.

$$max(Icc(j)') \geq min(Icc(j)') \quad (13)$$

$$Icc(j)-max(Icc(j)') \geq Idiv \quad (14)$$

$$min(Icc(j)')-Icc(j) \geq Idiv \quad (15)$$

3. Test generation

3.1 Test generation algorithm

Until now, test generation algorithms have not been proposed, which are based on supply currents of TTL circuits. Therefore, in this paper, we use a primitive test generation algorithm. The algorithm is based on fault simulation techniques[10], which is described below.

[1]Set j=0 and Nl=0.

[2]If Nl is greater than NL, stop this algorithm, where NL is a parameter to stop this algorithm.

[3]Generate an input vector(Tj) with random numbers and set j=j+1.

[4]By performing logic simulation, determine the logic value of each signal line for Tj.

[5]Insert a single fault at a signal line.

[6]Determine the logic value of each signal line and calculate the supply current of the circuit.

[7]If the supply current satisfies either (14) or (15), select the input vector as a test vector.

[8]If all faults which can be sensitized with Tj are not inserted, go to [5].

[9]If all faults have been detected, stop this algorithm.

[10]If Tj is not selected as a test vector, set Nl=Nl+1 and go to [2]. Otherwise, set Nl=0 and go to [3].

3.2 Test generation for TTL combinational circuits

We performed some experiments for evaluating our method. In our experiments, the benchmark circuits in ISCAS-85 are used as CUTs and NL is set to be 50. Since multi-input gates are used in the circuits, they are converted with the gates shown in Table 1.

In order to evaluate the effectiveness of our current testing, we derived test vectors for a conventional fault detection method, which is based on the logic values of the primary output terminals and is referred to "logic testing" in this paper. Both the open-circuit faults and the bridge faults with the Vcc lines can be modeled as stuck-at-1 faults. The bridge faults with the GND lines can be modeled as stuck-at-0 faults. Then, in order to derive test input vectors of the logic testing, an algorithm is used, which is modified so that at step [6] and [7] in section 3.1, the output logic values can be used in order to detect faults instead of the supply current.

Table 2 shows test generation results of our current testing and the logic testing. Each Idiv in Table 2 is determined by (7). From Table 2, it is found out that the size of test input vectors for the current testing is more reduced and the vectors are obtained quickly than the logic testing, except for C6288.

Faults can be detected by (14) and (15) if the supply current testing method is used. Therefore, the fault coverage depends on Idiv. Idiv is determined by the used A/D converter and the maximum value of Icc(j) of the unfaulty circuit. However, Idiv can be made smaller, if circuits are divided into some circuit blocks and the supply current of each circuit block is used for testing. Therefore, in Table 3, Idiv is set to be 0.1mA for each circuit. As shown in Table 3, by decreasing Idiv, the fault coverage can be improved and the test inputs can be derived more quickly. Furthermore, from Table 2 and 3, it is found out that the fault coverage of the current testing can be greater than the logic testing, except for C6288.

For C6288, the same fault coverage can be obtained by the current testing as the logic testing, while the size of the test vectors is increased and it takes more time to derive the test inputs than the logic testing. That is why the effects of faults on the supply current can be canceled by other gates. It is expected that it is more effective to detect faults by using a fault detection method based on both the supply current and the logic values of primary output terminals. Therefore, we examined the effectiveness by modifying the algorithm in section 3.1 so that if either the supply current or the output logic values are different from ones of the

Table 2 Test generation based on supply currents.

CUT	Idiv [mA]	Number of test inputs	Fault coverage [%]	CPU time [sec]
C19	0.004	5(8)	100(92.9)	0.1(0.2)
C432	0.053	45(73)	99.9(98.5)	$3.6\times10^{1}(1.1\times10^{2})$
C499	0.086	36(55)	98.3(97.6)	$5.9\times10^{1}(1.7\times10^{2})$
C880	0.111	56(96)	97.0(97.5)	$1.9\times10^{2}(4.3\times10^{2})$
C1355	0.123	72(88)	97.1(96.8)	$5.5\times10^{2}(1.1\times10^{3})$
C1908	0.201	54(146)	93.2(93.8)	$1.1\times10^{3}(1.1\times10^{4})$
C2670	0.348	62(89)	96.4(82.1)	$3.2\times10^{3}(1.3\times10^{4})$
C3540	0.416	89(214)	97.5(94.3)	$5.9\times10^{3}(2.6\times10^{4})$
C5315	0.650	122(191)	98.2(99.0)	$1.6\times10^{4}(2.1\times10^{4})$
C6288	0.620	162(49)	97.6(99.5)	$2.9\times10^{4}(4.2\times10^{3})$
C7552	0.881	173(213)	92.6(93.3)	$1.1\times10^{5}(1.4\times10^{5})$

The numbers in () are for test input vectors of logic testing.

Table 3 Test input vector for Idiv=0.1mA.

CUT	Number of Test inputs	Fault covarage [%]	CPU time [sec]
C880	54(-15)	97.1(+0.1)	1.8×10^{2} (-0.1×10^{2})
C1355	70(-2)	97.1(±0)	5.4×10^{2} (-0.1×10^{2})
C1908	52(-20)	94.0(+0.8)	8.9×10^{2} (-2.1×10^{2})
C2670	53(-9)	99.0(+2.6)	1.2×10^{3} (-2.0×10^{3})
C3540	82(-11)	98.4(+0.9)	$4.2\times10^{3}(-1.7\times10^{3})$
C5315	59(-64)	99.9(+1.7)	$3.6\times10^{3}(-1.2\times10^{4})$
C6288	63(-99)	99.5(+1.9)	$5.7\times10^{3}(-2.3\times10^{4})$
C7552	94(-77)	99.0(+6.4)	$1.3\times10^{4}(-9.7\times10^{4})$

The numbers of () are the differences from the test input vectors based on supply currents in Table 2.

unfaulty circuit, the circuit can be determined as a faulty circuit. The results are shown in Table 4. As shown in Table 4, the smaller size of test vectors can be derived by the method more quickly than either the current testing or the logic testing, and the fault coverage can be improved. Therefore, we think that it is very useful to measure both the supply current and the output logic values for testing.

It is impossible to insist that the current testing can derive its test vectors more quickly than the logic testing, since many algorithms for the logic testing that can derive test vectors more quickly are not used in these evaluations. The comparison of the CPU time remains as a future work. However, it is expected that test input vectors can be derived more quickly than the logic testing with the automatic observability.

Table 4 Test input vector based on supply current and output logic values

CUT	Number of Test inputs	Fault covarage [%]	CPU time [sec]
C19	5(±0)	100(±0.0)	0.1(±0)
C432	44(-1)	99.9(±0.0)	3.6×10^{1}(±0)
C499	36(±0)	98.3(±0.0)	6.0×10^{1}(+0.1)
C880	57(+1)	97.2(+0.2)	1.8×10^{2} (-0.1×10^{2})
C1355	70(-2)	97.1(±0.0)	5.4×10^{2} (-0.1×10^{2})
C1908	53(-1)	94.0(+0.8)	9.0×10^{2} (-0.2×10^{3})
C2670	54(-8)	99.0(+2.6)	1.2×10^{3} (-2.0×10^{3})
C3540	84(-5)	98.4(+0.9)	4.2×10^{3}(-1.7×10^{3})
C5315	112(-10)	99.7(+1.5)	7.5×10^{3}(-8.5×10^{3})
C6288	49(-113)	99.5(+1.9)	4.8×10^{3}(-2.4×10^{4})
C7552	156(-17)	98.7(+6.1)	3.0×10^{4}(-8.0×10^{4})

The numbers of () are the differences from the test input vectors based on supply currents in Table 2.

4. Conclusion

In this paper, test input vectors of TTL combinational circuits for the supply current testing are derived and the fault coverage is examined. As the result, it is checked that the supply current testing can detect more faults than the fault detection methods based on logic values of primary output terminals, and can reduce the number of test input vectors. Furthermore, the test vectors are generated for a fault detection method based on both the supply current and the primary output logic values, and it is shown that it is more effective to use both of them for testing circuits.

In this paper, our method has not been evaluated from the practical point of view. Practical evaluation of our method is one of the future works.

Acknowledgements

The authors appreciate the useful advice given in this study by Prof. Shuzo Yajima in Kyoto University.

References

[1]M.W.Levi: "CMOS is most Testable", Proc. of Int. Test Conf., pp.25-34(1982).

[2]J.M.Soden and C.F.Hawkins: "Test Considerations for Gate Oxide Shorts in CMOS ICs", IEEE Design & Test of Computers, pp.56-64,Aug.(1986).

[3]R.R.Fritzemeier,J.M.Soden and R.K.Treece: "Increased CMOS IC Stuck-at Fault Coverage with Reduced IDDQ Test Sets",Proc. of Int. Test Conf.,pp427-434(1990).

[4]Y.K.Malaiya and S.Y.H.Su: "A New Fault Model and Testing Techniques for CMOS Devices", Proc. of Int. Test Conf.,pp.25-34(1982).

[5]P.Nigh and W.Maly: "Test Generation for Current Testing", Proc. of European Test Conf.,pp.194-200(1989).

[6]T.Storey,W.Maly,U.J.Andrews and M.Miske: "Stuck Fault and Current Testing Comparison Using CMOS Chip Test", Proc. of Int. Test Conf. (1991).

[7]M.Hashizume et al.: "Fault Detection of Combinational Circuits Based on Supply Current", Proc. of Int. Test Conf., pp.374-380(1988).

[8]M.Hashizume et al.:"Fault Detection of TTL Combinational Circuits Based on Supply Current", Systems and Computers in Japan, Vol.22, No.10(1991).

[9]J.Galiay, Y.Crouzet and M.Vergniault: "Physical Versus Logical Fault Model in MOS LSI Circuits: Impact on Their Testability", Computers, Vol.C-29,No.6,pp.531-537.

[10]M.Abramovici, M.A.Breuer and A.D.Friedman: "Digital Systems Testing and Testable Design",pp.131-177, Computer Science Press (1990).