APPLICATION OF YIELD MODELS FOR SEMICONDUCTOR YIELD IMPROVEMENT

Daren L. Dance
SEMATECH, Austin, TX 78741

Richard Jarvis
AT&T Microelectronics, Orlando, FL 32819

Abstract

Yield models may be applied to increase the yield learning rate in semiconductor manufacture. Detailed equipment models can be used to predict the defect-limited yield from estimates of particles added per wafer pass. These general yield models may be refined to reflect specific processes, equipment, and design rules in more accurate critical area estimates. After validation, refined models can be applied to direct particle reduction and yield improvement efforts amid conflicting priorities. Yield improvements have been demonstrated by applying defect-limited yield models in a production manufacturing facility.

Introduction

As semiconductor technologies advance from generation to generation, manufacturing requirements become increasingly difficult. Defect density reduction is required as the complexity of semiconductor design and technology increases. Published defect density trends and forecasts indicate that for every three generations of technology, a defect density reduction of at least one order of magnitude is required [1]. Defect reduction efforts must focus on processes and equipment. Processes and equipment must be designed for minimum particles, assembled in a clean environment, installed correctly, and operated for minimum defect density.

Manufacturing improvements may be monitored by comparing unit price to cumulative manufacturing volume. These price-volume plots have been referred to as learning curves. Learning curves clearly show manufacturing improvement. But learning curves contain a fallacy: Increased production does not automatically cause unit price reduction as the learning curve implies. Blindly producing more and more of the same product in the same way does not increase productivity. Unit price reduction results from continuous improvement by applying knowledge gained from increased production.

0-8186-2837-5/92 $03.00 © 1992 IEEE

The Improvement Cycle

Applying Demming's Shewhart improvement cycle to all phases of the product life cycle results in continuous improvement [2]. Increased production provides increased opportunities to apply the Demming improvement cycle. Three ways of increasing the learning rate are:

1. Increase the production rate to increase improvement cycle opportunities,
2. Shorten cycle times to provide more frequent learning opportunities, or
3. Increase the learning rate from each improvement cycle.

A process improvement cycle using yield models has been described by several authors [3, 4, 5]. This cycle accelerates learning curve progress by implementing the yield model in a process improvement cycle. The specific yield model equation used is not critical to the improvement cycle. Thus, model selection is left to the user. The Seed's model is used for illustration purposes.

Semiconductor manufacturing can be divided into processing zones, each containing a photolithographic sequence. The yield model can be applied to the processing zone as well:

$$\overline{Y} = \prod_{i=1}^{k} \frac{1}{1 + AP_{fi}D_{0i}} \tag{1}$$

Defect data from the ith zone visual defect inspection estimates defect-limited yield for the ith processing zone.

Yield estimates for a lot from a defect-limited yield model may be compared to process capabilities using statistical process control methods, driving the process improvement cycle. This information can be fed back to prior processing to make engineering decisions for improving process, methods and equipment. Inspection, analysis, and feed back are repeated for each process zone.

After processing is finished, electrical test yield is compared with model yield forecasts. Analyzing these differences drives another improvement cycle. If failure analysis shows the presence of non-random defect related problems then information is fed back to the process. Otherwise yield model parameters are updated for continuous improvement.

The improvement cycle can be improved to accelerate learning by using detailed yield models. Rather than using a single defect density estimate to represent all defect mechanisms, detailed yield models characterize the contribution of each process zone or defect type to defect-limited yield. This is difficult and expensive, requiring estimates of defect distribution and fault probability by defect type. However, only detailed yield models trace yield losses to fundamental causes. Knowledge of cause and density by defect type allows focusing on significant problems first.

Equipment PWP Yield Model

A detailed equipment yield model can be used to predict defect-limited yield from estimates of particles added per wafer pass (PWP). Equipment particle counts are obtained by cycling bare wafers through the equipment, comparing before and after particle measurements made with a laser wafer surface particle counter to estimate particles added per wafer pass. An equipment level model assumes that defects within a zone are similar and can be added to generate a total PWP for each zone. The zone PWP defect density is factored by the fault probability and device critical area to estimate fault density. Knowing area and fault density allows calculating defect-limited yield for the zone:

(2)

$$\overline{Y} = \prod_{i=1}^{k} \frac{1}{1 + AP_{fi} \sum PWP_{zone_i}}$$

The equipment PWP yield model has several applications for yield improvement including:

- Identify process steps and equipment with large yield improvement impacts
- Study the yield impact of particle reduction plans
- Estimate the yields of new product designs, technologies, and design rules
- Statistically estimate PWP targets for new equipment
- Estimate the yield impact of transfering processes from one equipment set to another
- Assist in estimating lifetime cost of ownership for equipment

Application to Production

The equipment PWP yield model was developed at SEMATECH for their Phase 1 (0.8μm) process and was subsequently transferred for use by the SEMATECH member companies. To use the model, a company needed to customize the model to reflect their process and equipment set and tune the model to their design rules and the critical areas of their products. This refined model becomes a powerful tool for manufacturing yield improvement.

To fine-tune the model for acceptance by a member company's marketing and management, it was customized to reflect an improved knowledge of the design rules and critical areas of their specific products. This refined model reduces the error due to estimating critical areas and probabilities of failure. Within any device level, there are a number of pattern characteristics that contribute to critical area, both horizontal and vertical. For this model, only the horizontal characteristics have been considered, therefore model accuracy could be further improved to add vertical models for each interacting level.

Examples of device characteristics used to estimate critical area are:

- Metal to metal line space; all levels of metal
- Metal line width; all levels
- Polysilicon line space; all levels
- Polysilicon linewidth; all levels
- Gate oxide under polysilicon gates
- Contact areas; including:
  - metal to poly
  - metal to silicon
  - poly to silicon 'buried' contacts
- Field oxide isolation edges
- Spaces and widths of ion implanted areas

Horizontal characteristics that need to be considered include physical opens, shorts, and area contamination. Line to line spaces, line widths, and electrically active oxide and contact areas at critical defect sizes are just a few of the types of critical geometries that can be adversely effected by a defect. For each photoresist level, 1 to 6 critical design geometries were identified. The critical area for each geometry was determined for each product studied. These critical areas were totaled into a critical area per level which replaced the critical area in equation (2) determined by probability failure calculations. Since most pattern levels are, for the most part, isolated from each other, interaction between each level was keep to a minimum. As noted in equation (2), the defect densities from each process zone were matched to the critical areas per level and then applied to the yield equation, to estimate the defect-limited yield for each processing zone.

With the refined critical areas and production PWP data for each zone, yield model estimates varied less than ±8% of actual yields for one family of products and less than ±2% for another family. These estimates are well within the process yield confidence intervals. Yield model variation of ± 10 to 15% was expected for the unrefined version of the model.

Model Validation

The use of any model as a tool for yield prediction, must be preceded by validating the model to actual yield performance. Not only should this be done when first generating the model, but should continue throughout the use of the model. Many essential elements of the model, such as equipment set (batch vs. single wafer processing), critical areas, and process PWP values change with time and continuous improvement. A favorable feature of this model is that it operates on a personal computer level and can therefore be used by the manufacturing process engineers as changes occur.

Even with the improved predictability using refined critical areas, actual yield trends and variations are the starting point for model validation. This was done two ways, forward and backward. Forward uses the current trend of PWP from each tool group (based on usage, like nitride plasma etch or resist coating) to estimate

the yield for several products within a process/technology family and for different families. This estimate is compared to the actual yields for product manufactured during the period that the PWP data was taken. Table I shows the percent differences to actual product yields for the SEMATECH transferred model, the revised critical area model, and for comb and meander electrical short loop results. For many of these products, hundreds of wafers where manufactured during the validating period of over 6 months. Note that errors over ± 10% occur for the as-transferred SEMATECH Model and for electrical zone monitors since neither consider the actual critical areas relating to defect impact.

Table I: Yield Model Validation
Delta of Actual vs Predicted Yield

DEVICE	SEMATECH MODEL	CRITICAL AREA MODEL	ELECTRICAL ZONE MODEL
1.25 μm Process			
Product A	-5%	+2%	+2%
Product B	-7	+8	+7
Product C	+8	-3	+12
Product D	-18	-8	+4
0.9μm Process			
Product E	-20%	-2%	-12%
Product F	-5	-3	-15
Product G	+12	+7	+6
Product H		+4	

Backward validation involves working with Failure Analysis teams to determine when a positive or negative yield impact to a specific product has occurred that is particle related. Shortly after the forward validating period, just such an occurrence presented itself when a severe particle problem was found to affect some product wafers while others were unaffected during the same 90 day period. Failure mode analysis determined that particles were blocking the contact on metal 1 contacts to poly and source/drain active areas. In this case, a contact window oxide plasma etch tool developed a particle problem that was not detected with the PWP corrective action limits specified by manufacturing. Since only 1 of 4 etch tools was effected, this was a prime opportunity for model validation. The results are summarized in Table II.

Table II: Yield Model Validation
Contact Window Etch

	Product A	Product B
Validation: Std tools		
Model Predicted	38% ±8%	55% ±0%
Actual	36%	55%
Study: With bad tool		
Model Predicted	26% ±10%	36% ±10%
Actual	26%	50%

The model was first validated using the PWP data from only the unaffected window etch tools (standard processing). Product A averaged a yield of 38% during this period and the model predicted 36%. For Product B, 55% actual versus 55% predicted. The PWP data for the affected tool was then used to obtain 26% Product A and 36% Product B yield estimates. Product A did show a 26% yield for lots manufactured across that etcher, though Product B still showed about 50%. Examining the volume of lots processed, Product A had 4, about 200 wafers, while Product B only had about 50. Statistically, the Product A yield estimates are more accurate than Product B.

Model Application

After validation, the equipment PWP yield model was used to study the yield impact of particle reduction plans. Sensitivity analysis using the equipment PWP yield model identified the yield improvement of potential particle reduction by each process tool. This analysis tabulated the gain-in-yield estimate obtained if a PWP reduction of 50% were achieved for a tool and ranked the top tools requiring improvement. Table III shows two lists of equipment improvement priorities. The first is the yield model generated parieto with the left column indicating the key tool groups that need improvement in order. The right column shows the priority of tools if only PWP was considered. A process team from engineering, manufacturing, and maintenance group, chartered to reduce defects and improve yield, could work on any of these tools, but focused efforts on only those tools that really impacted yields, like those in the left column. The difference between the columns is due to considering the critical pattern geometries processed in those tools.

Table III: Equipment Improvement Parieto
February 1991

Yield Potential (Model)	PWP Reduction Potential
Poly/TaSi	High Pressure Oxidation
LPCVD Oxide	LPCVD Oxide
Wet Clean	Poly/TaSi
Resist Strip	PRS - 1000
Oxide Etch	Passivation Etch
Window Etch	Poly Etch
High Pressure Oxidation	Oxide Etch
Metal Etch	Window Etch
Implant	Wet Clean
Poly Etch	Passivation Deposition

Table IV: Equipment Improvement Parieto
Yield Improvement Potential

June 1991	September 1991
Window Etch	Wet HF Clean
Wet HF Clean	Oxide Etch
Oxide Etch	Wet Clean
Wet Clean	Batch Wet Processor
Resist Strip	Resist Strip
Metal Etch	Metal Etch
Poly/TaSi	Poly/TaSi
Batch Wet Processor	Al Deposition
Al Deposition	High Pressure Oxide
High Pressure Oxide	Window Etch

As changes occurred, regular maintenance of the model was done. In June of 1991, a new study was done, and then again in September. These are shown in

Table IV. As can be seen, the list of tools has changed since the initial February study. Resource directions should be changed, as required, to maximized yield improvement. As can be seen in the 6/91 parieto, oxide window etch still hit high on the list, similar to the backward yield example during validation. During the period of 6/91 to 9/91, new processing tools completed qualification and window etch was dedicated to these new tools. As is then seen on the 9/91 parieto, window etch then dropped markedly down the list versus LTO oxide etch, which was still being done in the older tools.

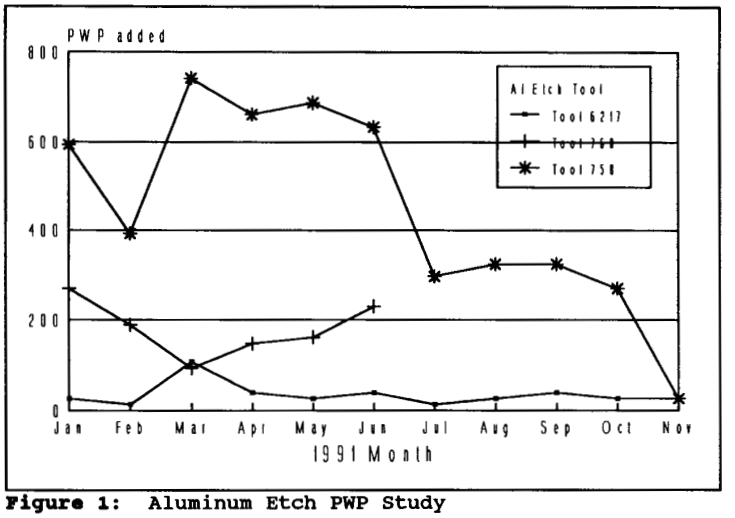

Figure 1: Aluminum Etch PWP Study

During these studies, all manufacturing tools were operating within specified limits. Any tool exceeding those limits for the routine monitors, was not used by production until corrective action resulted in passing PWP monitors. One question is, of course, what of the product that was manufactured in that tool before the monitor detected failure? To address this, tool vs tool studies were undertaken to find tool groups that had inconsistent individual tools within them, again like the window etcher example, but on a lower and ongoing scale.

Aluminum metal etch was just such a tool set, effecting two levels of metal patterning. The timeline plot, shown in Figure 1, shows the history of three plasma metal etching tools. The manufacturing facility where these etchers are has all PWP monitor data uploaded onto a mainframe database. This data includes all particle size distribution, type of monitor taken, tool the data was generated from, etc., and has this data for years of individual tool usage. This allows for data analysis on thousands of points, reducing the need for statistical analysis. During

early June, the PWP modeling indicated that the metal etch tools where impacting yield. Analysis of the individual tools found that tool 758 had a 5 to 6X higher particle count history, when all the data was examined. The impact to this tool was that it was not available to manufacturing 30 to 50% more often, cutting capacity. An additional study of the data showed that the particle distribution for any size evaluated was bimodal. With this knowledge, it was found that the wafers used for PWP monitoring were not placed consistently in the etcher. Examination of the worst particle site found partially hidden, corroded mechanical parts. When corrected, the PWP trend returned to that of the other similar tool, tool 768. As a result, capacity improved on tool 758, as well as the predictability of particles added during the etching process, an improvement very hard to quantify.

Ongoing 'best vs worst' tool studies occur on a routine basis. Each functional area of wafer manufacturing has key tools chosen from the model's tool group analysis. Recent studies of this type indicate the priority for improvement shown in Table V.

Table V: Tool Improvement Priority
Best vs Worst Tool Studies

Tool	Relative Priority
Wet Chemical Clean	2.5
Metal Etch, Old models	2.3
Low Current Implant	1.8
Resist Coat	1.4
High Current Implant	1.2
Thermal Oxidation	1.2
Contact Window Etch	1.1
Metal Etch, New models	1.0

As each tool within that group is modeled, the estimated yield delta for best versus worst tool is indicated. Improvement actions are then prioritized and a list of key actions is documented.

Long Term Impacts

Based on this priority setting methodology, implemented in early 1991, aggressive programs of particle reduction have resulted in significantly reduced particle levels as illustrated in Figure 2 (relative device/product defect densities as calculated from product yield) and improved yields. It is for this purpose, that particle per wafer pass (PWP) reductions should target reduced particle variation which leads

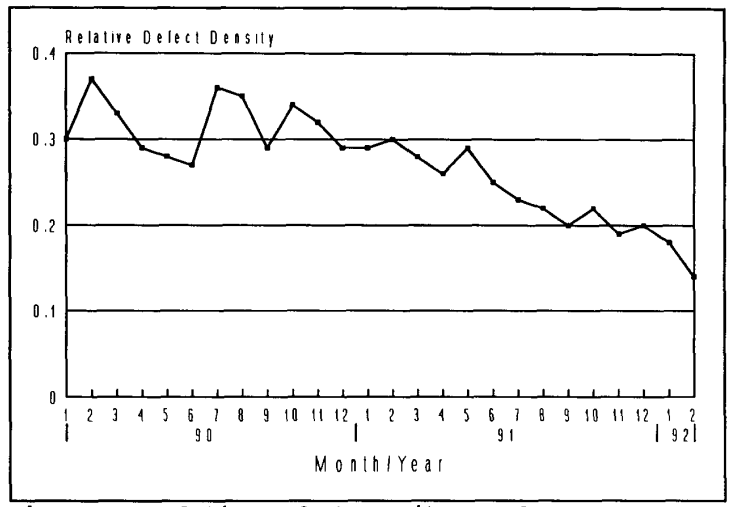

Figure 2: Relative Defect Density Trend

to reduced yield variation. Yield estimates based on modeling can direct resources to improve inconsistent situations in the most timely manner. As an additional benefit, reduction in yield variation allows for further tuning of the model parameters to increase yield estimation accuracy.

References

1. D. L. Dance, "Meeting Future Defect Density Requirements for Microelectronics," Electrochemical Society, Fall 1992, invited paper.
2. W. E. Demming, *Out of the Crisis*, Massachusetts Institute of Technology, Center of Advanced Engineering Study, Cambridge, Mass., 1986, p. 88.
3. C. H. Stapper, et al., "Evolution and Accomplishments of VLSI Yield Management at IBM," *IBM Journal of Research and Development*, September 1982, Vol. 26, No. 5, pp. 532-545.
4. R. A. Maeder, F. W. Oster, R. J. Soderman, "Semiconductor and Integrated Circuit Device Modeling," U. S. Patent 3,751,647, 1973.
5. S. Dimitrijev, N. Stojadinovic, Z. Stemenkovic, "Yield Model for In-Line Integrated Circuit Production Control," *Solid-State Electronics*, 1988, Vol. 31, No. 5, pp. 975-979.