In his keynote last month at Micro-45, Charles Webb said that I/O is a key issue for performance and that optical interconnect is attractive. Alas, he also cautioned that optical interconnect is always two generations away. This issue of *IEEE Micro* digs deep into the underlying technologies for optical interconnect to give a better understanding of what is possible and what still holds us back. Guest Editors Jeffrey Kash and Raymond Beausoleil have done a fine job of recruiting papers that span the broad range of issues with optical interconnect.

I am optimistic, so I think it is also useful to consider what we would do if optical interconnect is indeed available and practical in two generations? One result is that I/O and memory bus power would likely be reduced significantly, allowing us to either use that budget for other things or to reduce overall system power requirements. Since frequency has been power limited for many years, could we see a one-time bump in processor frequencies?

Database performance is highly dependent on fast I/O. Historically, much of that has been to and from disk. However, a combination of optical interconnects and flash memory could make databases compute bound instead of I/O bound. Would transactional memory take on vastly improved importance as a direct implementation mechanism for transactions in OLTP (online transaction processing), thus exploiting the new transactional capabilities appearing in a number of recent processors? Would new in-memory databases take on new importance?

Many graphics processing workloads and processors have huge bandwidth requirements and memory footprints. Could some of the memory on GPUs be replaced by additional compute capability, and leverage higher bandwidth access to a larger amount of memory? Will better bandwidth and larger flash-based memory yield more immersive games?

In data-center cloud environments, better bandwidth from optical interconnect could facilitate faster switching between virtual images and movement of virtual images between clusters, thus allowing more balanced use of resources and fewer of them, thus further reducing energy demands. Such fast switching could in turn place new demands on processor caching of instruction, data, and translation contexts.

There are doubtless many other changes in microarchitecture and beyond that will be enabled by improvements built on the optical interconnect ideas described in this issue. I hope that this issue will help you be prepared to use and develop those changes.

Happy reading!

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