Guest Editors’ Introduction

TOP PICKS FROM THE 2011
COMPUTER ARCHITECTURE
CONFERENCES

As guest editors of this IEEE Micro special issue and co-chairs of the selection committee, it’s our pleasure to introduce the ninth annual edition of IEEE Micro’s Top Picks from the Computer Architecture Conferences. In recent years, Top Picks has rapidly become a tradition in the computer architecture community, an important recognition of research excellence, and a great opportunity to take a step back and look at our field, by providing a high-level snapshot of some of the most influential research in one place.

Working with Editor in Chief Erik Altman, we followed our predecessors’ path and focused our attention on identifying publications that have high potential for long-term impact on computer architecture, in terms of either industry products or future research directions.

Selecting a dozen papers from the large body of high-quality research that our community produces is a challenging endeavor, and this year was no different. Despite the uncertainties of an imperfect review process, with the help of 30 distinguished members of our community, we selected articles that represent the current state of leading research in computer architecture.

The selection process

To help the review process, we asked authors to submit a three-page summary highlighting the novelty and impact of the work, in addition to a copy of the original conference paper. Although there was no constraint regarding the publication venue (as long as it was published in 2011), 35 percent of the papers came from ISCA, 29 percent from Micro, 14 percent from HPCA, and 9 percent from ASPLOS. We also had a smaller representation from Sigmetrics, DSN, DATE, ICPP, ICS, SC, NOCS, and PLDI.

This year we took a different position than in the past concerning submission rules, and decided that the guest editors would not be eligible to submit their work. We believe this better matches our community practices and improves the fairness of the selection process.

We received 77 submissions, in line with previous years, for which we requested four reviews by the 30 selection committee members (see the “Selection Committee” sidebar). Each member was responsible for nine to 10 articles. In the spirit of cloud computing, the review system, based on the open source HotCRP software, was hosted on hpcloud.com and managed by Paolo Faraboschi.

Paolo Faraboschi
Hewlett-Packard Labs

T.N. Vijaykumar
Purdue University
We significantly revised the review form by encouraging qualitative assessments of the publication’s potential impact. For example, we highlighted questions such as, “Is the problem being studied important and yet to be solved?” and “In the past five years, has the problem received much attention? What about the next five years?” and “What are the chances of the paper having long-term impact and fostering follow-up research?” For the overall merit score, we asked each committee member to rank-order the papers assigned to him or her, instead of giving absolute “accept/reject” scores. This ranking helped normalize the scores across different reviewers, whose notions of accept or reject could vary significantly. We ensured that at least the top two papers from each reviewer were discussed at the meeting. These changes significantly helped us group the papers and identify the candidates for the final discussion.

More than 80 percent of the committee members attended the online meeting on January 7, 2012, which was supported by a combination of technologies, including shared spreadsheets, virtual rooms, and audio connection. Committee members with a conflict of interest regarding a paper being discussed left the audio call and were notified when they could rejoin. Through an extensive offline discussion among the committee members and the guest editors before the PC meeting, we identified a short list of 46 submissions that were individually discussed at the meeting and from which we selected the final 12 Top Picks papers of 2011.

The 2011 Top Picks articles

For this year’s Top Picks issue, we include 12 articles that demonstrate the breadth and depth of ongoing computer architecture research (see the “Top Picks of 2011” sidebar). These articles fall into four themes. The first and largest theme is about architecting, connecting, designing, and programming many-core processors. In “KiloTM: Hardware Transactional Memory for GPU Architectures,” Wilson W.L. Fung et al. propose a hardware transactional memory extension to GPUs to ease expressing synchronization among thousands of threads, which makes up for the lack of multicore cache coherence in GPUs via a speculative transaction validation mechanism and a novel bloom filter structure. The Kilo-NOC architecture proposed by Boris Grot et al. (“A QoS-Enabled On-Die Interconnect Fabric for Kilo-Node Chips”) targets scalability and advances today’s state of the art by co-optimizing topology, flow control, and quality-of-service mechanisms in a drive for efficiency. The Vantage cache...
The second largest theme deals with advances in memory technology. In "Active Low-Power Modes for Main Memory with MemScale," Qingyuan Deng et al. address the problem of main memory accounting for a growing fraction of server power and introduce active low-power modes, which trade bandwidth for energy savings while tightly limiting the associated performance impact. "Supporting Very Large DRAM Caches with Compound-Access Scheduling and MissMap" by Gabriel H. Loh and Mark D. Hill investigates stacked DRAM caches with conventional block sizes, introduces a scheduling mechanism that makes hits faster by exploiting DRAM row buffers, and accelerates misses by eschewing some stacked-DRAM accesses through a separate miss map. The Free-p work by Doe Hyun Yoon et al. ("Free-p: A Practical End-to-End Nonvolatile Memory Protection Mechanism") remaps worn-out nonvolatile memory blocks at a fine granularity without requiring large dedicated storage by embedding pointers to the remapped locations in the worn-out blocks, protects against hard and soft errors, and can be extended to chipkill.

The third group of articles explores scale-out computing issues. The work by Jason...
Mars et al. ("Increasing Utilization in Modern Warehouse-Scale Computers Using Bubble-Up") improves performance by colo-
cating mutually compatible applications on a single machine, which is critical for improving utilization in modern warehouse-scale computers. In "Optical High-Radix Switch Design," Nathan Binkert et al. propose a novel high-radix switch architecture that uses emerging integrated optical interconnect technology to reduce power by tailoring every switch component to best exploit optics, thus improving switch scalability and energy efficiency.

The last theme presents interesting per-
spectives on computer architecture trends by looking back and looking forward. In "What Is Happening to Power, Performance, and Software?" Hadi Esmaeilzadeh et al. analyze measured power and performance of a large variety of processors and workloads to better understand the combined effects and interactions of the rise of parallel processors and managed programming languages in the past decade. In "Dark Silicon and the End of Multicore Scaling," Hadi Esmaeilzadeh et al. highlight a crucial impending problem where future multicore chips will be power-limited to the point that an increasing fraction of cores will have to be kept powered off ("dark") at every new technology generation.

We hope you find the articles interest-
ing, and we welcome your feedback on the special issue. We encourage you to read the original conference versions of the articles in this issue.

Acknowledgments

We acknowledge several individuals who contributed to this special issue of IEEE Micro. Editor in Chief Erik Altman constantly guided us throughout the process. The authors sent us their high-quality submissions, which made our effort particularly challenging, but we are glad that they did! The selection committee members did an outstanding job in meeting the schedule, delivered thorough reviews, and profession-
ally and constructively discussed their perspectives to rapidly reach consensus at the final meeting.

Paolo Faraboschi is a distinguished tech-
nologist in the Intelligent Infrastructure Lab at Hewlett-Packard Labs. His research interests are at the intersection of computer architecture and systems and software, and include energy-efficient servers, system-on-chip architectures, modeling and simulation, and very long instruction word (VLIW) cores and compilers. Faraboschi has a PhD in electrical engineering from the University of Genoa.

T.N. Vijaykumar is an associate professor in the School of Electrical and Computer Engineering at Purdue University. His research is in computer architecture, focusing on performance, power, programmability, and reliability of general-purpose microprocessors and systems, including multicores and datacenter-scale clusters; power and performance optimizations for Internet router hardware; and architectures and compilers for software-programmable microfluidics. Vijaykumar has a PhD in computer science from the University of Wisconsin–Madison.

Direct questions and comments about this article to Paolo Faraboschi at paolo.faraboschi@hp.com or T.N. Vijaykumar at vijay@ecn.purdue.edu.

Selected CS articles and columns are also available for free at http://ComputingNow.computer.org.