A year ago, the 36th International Symposium on Computer Architecture featured the latest installment of the Computer Architecture Research Directions workshop. CARD is a series of minipanels, in which two experts take somewhat opposing viewpoints on important topics related to the future of computer architecture, under the direction of a moderator. As in previous years, attendees flocked to the CARD workshop to hear these debates. Two years ago, we featured a special issue on the 2007 CARD workshop. That issue generated favorable comments from Micro’s readership, so we decided to do it again. In this issue, we feature two articles derived from those minipanels, followed by two excellent general-interest articles.

In the first article, “The Future of Architectural Simulation,” Doug Burger and Joel Emer, under the direction of moderator James Hoe, debate the future of computer architecture simulation. They address issues such as simulator speed and the role of field-programmable gate arrays, but also tackle some interesting broader questions. For instance, does the limited scope of an architectural simulator lead to incremental research? And, can we devise shared research infrastructures that encourage academics to think long term, on a 10-year horizon?

In the third article, “Fine-Grained Activation for Power Reduction in DRAM,” Elliott Cooper-Balis and Bruce Jacob make a clever observation about the posted-CAS (column-address strobe) command and synchronous DRAM power savings. A posted-CAS command simplifies memory scheduling by being issued immediately following the activate command. Since posted-CAS makes the column addresses available to the SDRAM before they are needed, a subset of these addresses can be used to select a vertical subset (a partial row) of the selected bank in advance of column bit selection. A significant advantage of this power-saving approach is that it requires no changes to the standard SDRAM interface.

Finally, “Tuple Pruning Using Bloom Filters for Packet Classification,” by Hye-sook Lim and So Yeon Kim, addresses the important problem of packet classification at wire speed in network routers. Previous approaches, such as tuple space pruning, require multiple accesses to off-chip memory. The authors address this performance bottleneck through the use of several on-chip Bloom filters that reduce the number of unnecessary off-chip memory accesses. The approach is shown to outperform several previous approaches on multiple metrics.

I hope you enjoy these articles as much as I did. I always welcome your feedback at albonesi@csl.cornell.edu.

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