Welcome A-Board

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With this issue, I have the honor of welcoming six new members to the IEEE Micro Editorial Board: Alper Buyuktosunoglu, Kris Flautner, Steve Keckler, Norm Jouppi, Margaret Martonosi, and Shubu Mukherjee. Rather than write something about each of them, I’ll let the biographies of this distinguished group of industry and academic leaders speak for themselves (see the sidebar). I am truly humbled that they accepted my invitation to join the Board.

Coming up in our last issue of 2009 is a new column. This column will feature brief tutorials, but not in the traditional sense of “this is how this thing works.” Rather, the column is part tutorial, part opinion piece. I invite you to check it out. Coming in 2010 is a second new column and, after Top Picks and Hot Chips, issues on computer architecture debates and datacenter computing.

Here’s a brief introduction to the five articles in this general interest issue. They cover a wide range of subjects of interest to the Micro community: multicore computer architecture, benchmark analysis, real-time operating systems (RTOSs), test, and security.

Our cover feature article, “Dynamic Multicore Resource Management: A Machine Learning Approach,” by José Martínez and Engin Ipek, introduces a novel machine learning strategy to effectively manage shared resources in multicore microprocessors. The authors advocate a departure from conventional heuristic-based policies in favor of a new direction in which the architect specifies the objective function and determines the most appropriate machine learning approach and the variables to be considered. The authors demonstrate through two case studies that the resulting self-optimizing system achieves far better performance than current state-of-the-art control policies.

In the second article, “A Benchmark Characterization of the EEMBC Benchmark Suite,” by Jason Poovey, Thomas Conte, Markus Levy, and Shay Gal-On present a detailed evaluation of EEMBC, a popular benchmark suite for embedded microprocessors. Vendors often rely on standard benchmark results to assess the most suitable microprocessor for their particular applications. However, it’s difficult in practice to know which standard benchmarks are most representative. The authors present a methodology for benchmark characterization that exposes a program’s key attributes, and they demonstrate their approach using the EEMBC suite.

Tran Nguyen Bao Anh and Su-Lim Tan provide an in-depth analysis of RTOSs for embedded processor systems in their article, “Real-Time Operating Systems for Small Microcontrollers.” The authors provide a broad comparison of 14 RTOSs using criteria such as scheduling approach, system call/API support, and documentation. From this list, they identify four RTOSs with particularly rich system API support, and quantitatively compare them on an embedded platform, using oscilloscopes and logic analyzers to make accurate timing measurements.

Next, in “Memory Built-In Self Test in Multicore Chips with Mesh-Based Networks,” Hsiang-Ning Liu, Yu-Jen Huang, and Jin-Fu Li propose a memory built-in self test (BIST) approach suitable for multicore chips with packet-based networks. Because multicore chips have identical memories situated throughout the die, a single BIST circuit can broadcast test packets through the network to multiple memories, thereby achieving parallel test with lower overhead than dedicated BIST circuits. The authors describe the required network-on-chip support for their parallel BIST technique, and show that their implementation achieves modest overhead with fast test speeds.

The last article, “Hardware-Software Codesign for High-Speed Signature-Based Virus Scanning,” by Ying-Dar Lin, Po-Ching Lin, Yuan-Cheng Lai, and Tai-Ying Liu, describes their BFAST* scanning engine and its integration with Clam AntiVirus. The BFAST architecture searches in sublinear time by querying Bloom filters to derive the shift distance in the search window. The article describes the modules that BFAST* offloads from ClamAV and the communication interface. By implementing their system on a field-programmable gate array platform, the authors identify the performance bottlenecks and propose remedies for future work.

I hope you enjoy these articles, and I always welcome your feedback at albonesi@csl.cornell.edu.

Dave Albonesi
Editor in Chief
IEEE Micro
IEEE Micro welcomes six new members to its editorial board.

Alper Buyuktosunoglu is a research staff member in the Reliability and Power-Aware Microarchitecture Department at the IBM T.J. Watson Research Center. He has been involved in research and development work in support of IBM p-series and z-series microprocessors in the areas of power-aware computer architectures, dynamic power management, and high-level power modeling. His research interests are in the areas of high-performance, low-power, complexity-aware computer architectures, and power-performance modeling of microprocessors. Buyuktosunoglu has more than 25 pending or issued patents, has published more than 25 papers, and has served on various conference technical program committees. He has received several Invention Plateau Awards, a High Value Patent Application Award, a Research Technical Group Award, and an Outstanding Technical Achievement Award from IBM. Buyuktosunoglu has a PhD in electrical and computer engineering from the University of Rochester. He is a senior member of the IEEE.

Stephen W. Keckler is a professor of both computer sciences and electrical and computer engineering at the University of Texas at Austin. He is an Alfred P. Sloan Research Fellow, the 2003 winner of the ACM Grace Murray Hopper award, a recipient of an NSF CAREER award, and a winner of the 2007 President’s Associates Teaching Excellence Award at UT-Austin. His research interests include computer architecture, parallel processors, high-performance computing, VLSI design, and the relationship between technology trends and computer architectures. He coleads the UT-Austin TRIPS project, which has developed and prototyped high-performance adaptive computer systems. As codirector of the Computer Architecture and Technology (CART) Laboratory, Keckler’s research has been supported by DARPA, the US National Science Foundation, IBM, and Intel. He has a BS in electrical engineering from Stanford University and an MS and a PhD in computer science from the Massachusetts Institute of Technology. Keckler is a senior member of the IEEE and the ACM, and a member of Sigma Xi and Phi Beta Kappa.

Krisztian Flautner is the vice president of research and development at ARM Ltd. ARM designs the technology that lies at the heart of advanced digital products, with more than 15 billion processors deployed by mid-2009. He leads a global team that focuses on the understanding and development of technologies relevant to the proliferation of the ARM architecture. The group’s activities cover a wide breadth of areas, ranging from circuits, through processor and system architectures, to tools and software. Key activities are related to high-performance computing in energy-constrained environments. Flautner has a PhD in computer science and engineering from the University of Michigan, where he is currently a visiting scholar. He is a member of the ACM and the IEEE.

Norman P. Jouppi is a Fellow and director of the Exascale Computing Lab at HP Labs. He is known for his innovations in computer memory systems, including stream prefetch buffers, victim caching, multilevel exclusive caching and development of the CACTI tool for modeling cache timing, area, and power. He has also served as principal architect and lead designer of several microprocessors, contributed to the architecture and design of graphics accelerators, and extensively researched video, audio, and physical telepresence. His recent work includes implications of emerging nanophotonic technology on computer systems. Jouppi has an MS from Northwestern University and a PhD from Stanford University, both in electrical engineering. While at Stanford, he was one of the principal architects and designers of the MIPS microprocessor. Prior to joining HP in 2002, Jouppi was a staff fellow at Compaq Computer Corporation’s Western Research Laboratory in Palo Alto, California. He currently serves as past chair of ACM Special Interest Group on Computer Architecture (SIGARCH), is on the ACM Council and on the Computing Research Association (CRA) board. He holds more than 35 US patents and has published more than 100 technical papers, with several best paper awards and one Symposium on Computer Architecture (ISCA) Influential Paper Award. He is on the editorial boards of Communications of the ACM and IEEE Computer Architecture Letters, and is a Fellow of the ACM and the IEEE.
Margaret Martonosi is a professor of electrical engineering at Princeton University and an affiliated faculty member in Princeton’s Computer Science Department. From 2005–2007, she was associate dean for student affairs for Princeton’s School of Engineering and Applied Science. Martonosi’s research interests are computer architecture and the hardware/software interface, with particular focus on power-efficient systems and mobile computing. In the field of processor architecture, she has done extensive work on power modeling and management and on memory hierarchy performance and energy, including the development of the Wattch power modeling tool, the first architecture-level power modeling infrastructure for superscalar processors. Her memory hierarchy work has included early performance-oriented studies, as well as more recent work on energy-aware memory hierarchies. In the field of mobile computing and sensor networks, Martonosi led the Princeton ZebraNet project, which established the field of sparse, mobile sensor networks and demonstrated effectiveness through two real-world deployments on plains zebras in Kenya. She is coleader of the Sarana project, which is building software interfaces for collaborative computing among mobile devices. She recently completed two terms as vice-chair of the ACM Special Interest Group on Computer Architecture (SIGARCH) and is now on the SIGARCH Board of Directors. Martonosi has coauthored more than 100 refereed publications and a technical reference book on power-aware computing, and is an inventor on five granted US patents. She has a bachelor’s degree with distinction from Cornell University and master’s and PhD degrees from Stanford University, all in electrical engineering.

Shubu Mukherjee is a principal engineer and director of Intel’s Simulation and Pathfinding of Efficient and Reliable Systems group. The SPEARS group spearheads architectural change and innovation in the delivery of enterprise processors and chip sets by building and supporting simulation and analytical models of performance, power, and reliability. Mukherjee is widely recognized as an expert on architectural design for soft errors. He has made pioneering contributions toward architectural vulnerability modeling for soft errors, redundant multithreading techniques, the design of Intel’s System Environment Monitoring Agent, the creation of the performance-modeling infrastructures Cameroon (jointly with a team of Intel engineers) and Asim (jointly with Joel Emer), the design of the Alpha 21364 interconnection network, and the creation of the first shared memory prediction scheme. He won the 2009 Maurice-Wilkes award for his work on soft errors. He was the general chair of ASPLOS in 2004. He has co-authored more than 40 external papers and the book, Architecture Design for Soft Errors (Elsevier 2008). He holds 23 patents and has filed another 25 more in Intel. Mukherjee is an associate editor of IEEE Transactions of Secure and Dependable Computing (TDSC) and serves on the IEEE Computer Architecture Letters editorial board, US National Science Foundation (NSF) panels, numerous technical program committees, Intel Corporation’s patent committee, and the Board of Trustees of Merrimack Repertory Theatre. Mukherjee has a BTech. from the Indian Institute of Technology, Kanpur, where he serves as an adjunct faculty. He has an MS and a PhD from the University of Wisconsin-Madison. He is a Fellow of the IEEE.
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