This special issue marks *IEEE Micro*’s fourth annual publication of Top Picks from the Computer Architecture Conferences. This tradition, initiated by *IEEE Micro*’s former Editor in Chief, Pradip Bose, has become a key event in the computer architecture community. In this very dynamic field, every year, several highly reputed conferences attract the most interesting research works. This issue showcases some of the most relevant works presented at these conferences and published in their proceedings. Choosing these papers was a very difficult task, given that we had to choose among a large number of high-quality submissions that had already gone through a very selective review process for their respective conferences. The selection criteria put special emphasis on the novelty of the work and its potential impact on industry. We interpreted industry relevance in a broad sense, including short-term and long-term potential impact. Selecting only 11 papers among the many excellent submissions was a tough job; space restrictions prevented the publication of many other outstanding papers.

**The submissions**

For each submission, we requested a three-page summary that included an overview of the work, an explanation of its novelty, and a discussion of its relevance to and impact on architects and designers of current and future-generation computing systems.

We received 76 submissions, corresponding to papers from several conferences held in 2006:

- 23 papers from the International Symposium on Microarchitecture (Micro),
- 19 papers from the International Symposium on Computer Architecture (ISCA),
- 15 papers from the International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS),
- 7 papers from the International Symposium on High-Performance Computer Architecture (HPCA),
- 5 papers from the International Conference on Parallel Architectures and Compilation Techniques (PACT),
- 3 papers from the International Conference on Computer Design (ICCD),
- 2 papers from the International Conference on Dependable Systems and Networks (DSN),
- 1 paper from the International Workshop on Rapid System Prototyping (RSP), and
- 1 paper from the International Symposium on Computer
Architecture and High Performance Computing (SBAC-PAD).

More than 90 percent of the submissions came from five leading computer architecture conferences: Micro, ISCA, ASPLOS, HPCA, and PACT.

The reviewers

To review the submissions, we assembled a program committee of 31 highly respected architects in our community from both industry and academia:

- Sarita Adve, University of Illinois
- David Albonesi, Cornell University
- Pradip Bose, IBM
- David Brooks, Harvard University
- Doug Burger, University of Texas, Austin
- Brad Calder, Microsoft and University of California, San Diego
- Doug Carmean, Intel
- Calin Cascaval, IBM
- Tom Conte, North Carolina State University
- Jose´ Duato, Universidad Polite´cnica de Valencia
- Joel Emer, Intel
- Babak Falsafi, Carnegie Mellon University
- Dirk Grunwald, University of Colorado, Boulder
- Mark Hill, University of Wisconsin
- Wen-mei Hwu, University of Illinois, Urbana-Champaign
- Lizy John, University of Texas, Austin
- Norman P. Jouppi, HP Labs
- Konrad Lai, Intel
- Kai Li, Princeton University
- Kathryn McKinley, University of Texas, Austin
- Scott A. Mahlke, University of Michigan, Ann Arbor
- Chuck Moore, AMD
- Jaime Moreno, IBM
- Trevor Mudge, University of Michigan, Ann Arbor
- Yanos Sazeides, University of Cyprus
- John Shen, Nokia Research Center
- Michael D. Smith, Harvard University
- Dean Tullsen, University of California, San Diego
- Bob Valentine, Intel
- T.N. Vijaykumar, Purdue University
- Victor Zyuban, IBM

These committee members’ dedication and professionalism were key factors in the selection process.

We assigned each paper to four or five members of the program committee, and each member was asked to review about 12 papers. In total, we requested 314 reviews, and we received all of them without exception—yet another indication of the committee members’ high professionalism.

All members attended the day-long program committee meeting in Chicago on 5 November 2006. During that meeting, every committee member had access to all information for every paper except those with which she or he had a conflict of interest. This information included the short and long versions of the submitted papers, the reviews, and the reviewer identities. Having all the reviewers on site allowed for a very rich discussion, in which everybody had the opportunity to comment and to justify their viewpoints. The discussion was open to all committee members except those who had a conflict of interest with the work under consideration; members were requested to leave the room during the discussion and decision process for papers with which they had conflicts.

The selections

For this year’s Top Picks issue, the committee selected 11 papers covering some of the most active research areas in computer architecture (see the sidebar, “Top Picks of 2006”). The mix of topics in this year’s issue is definitely different from those of previous years, demonstrating shifting trends in computer architecture.

About one-third of the papers selected deal with the design of resilient computing systems, an area that has attracted strong attention lately in our research community and has sprouted many research activities in industry and academia. Top Picks includes articles addressing detection of and recovery from both hardware and software errors, using several novel, interesting approaches. The first article, by Sarangi et al., presents
...use an emerging technology, 3D stacking, to provide a cost-effective introspection system. The article by Eyerman et al. presents a scheme for quantifying the contribution of the main microarchitectural components to the achieved performance.

Another two articles address the design of general-purpose processors. Kim et al. propose a scheme for dynamic predication; and Sha, Martin, and Roth present a novel approach to implementing dynamic memory disambiguation logic.

Finally, the last article, by Lin et al., presents a programmable architecture for wireless protocols.

We hope you enjoy reading these articles, and we encourage you to read the original works as well. We welcome your feedback on this year’s Top Picks and any suggestions on how to improve the special issue for the future.

Acknowledgments

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Ronny Ronen is an Intel Senior Principal Engineer and director of Intel’s Microprocessor Research Lab in Haifa, Israel, focusing on microarchitecture research. Ronen has been with Intel for more than 25 years. He was heavily involved in the definition stages of the Intel Pentium M processor and its successors; earlier he led compiler and performance simulation...
activities in the Software Department of Intel Israel. Ronen received his MSc degree from the Technion, Israel Institute of Technology. He is a senior member of the IEEE.

Antonio González is the founding director of the Intel-UPC Barcelona Research Center and a professor of computer architecture at Universitat Politècnica de Catalunya. His research focuses on computer architecture, with particular emphasis on processor microarchitecture and code generation techniques. González is an associate editor of IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems, ACM Transactions on Architecture and Code Optimization, and Journal of Embedded Computing.

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