As guest editors, we are pleased to present in this issue of *IEEE Micro* a collection of the best-of-the-best articles based on the most exciting and interesting presentations at the Hot Chips 17 conference held last August at Stanford University.

Hot Chips’ focus is providing timely technical information on important, upcoming, or previously unreported chips and related technologies. The conference is unusual because it’s a technical conference that’s product focused. The conference is not about research, although a typical Hot Chips conference does have some research presentations. And, it’s (especially) not about marketing. In general, Hot Chips’ bias has been toward chips and related technologies that are not only “hot” (or in the case of low power, “cold”), but also interesting at the architectural level.

To accomplish this, Hot Chips runs differently from other conferences in three ways. First, unlike most technical conference programs, Hot Chips’ program is not assembled completely from articles that come in over the transom (or past our spam filter). In addition to considering unsolicited submissions, we also actively solicit presentations that meet our criteria.

Second, presentations for Hot Chips are accepted on the basis of an abstract, and the proceedings only contain copies of the speakers’ slides so presenters can show their latest work with the least possible effort and shortest lead time. This bleeding edge focus can also result in articles that must be withdrawn when marketing and product schedule realities interfere. This year was unusual: No one dropped out of the conference.

Finally, although we provisionally accept presentations on the basis of an abstract, we don’t fully accept them until a program committee member (usually the session chair) reviews and approves the slides for clarity and sufficient technical content. Hot Chips session chairs are not merely decorative.

Industry (and conference) trends

Like any conference, Hot Chips tracks the trends in its field—in this case the semiconductor, electronics, and computer industries. This year, as usual, the conference featured some high-end CPUs, including those destined for PCs and game machines. Several presentations also focused on the prime industry concern of minimizing and managing power.

As always, some talks covered specialized processors for application domains, such as audio, video, and communications that are believed to be large enough to support specialization and to require the level of performance that is only available from specialized designs.

We made a special effort this year to attract presentations from the field-programmable gate array world, which has been underrepresented at previous Hot Chips conferences. The program was also salted with presentations on cutting edge and speculative technologies.

It’s interesting to observe Hot Chips’ evolution. The conference started with a focus on high performance CPUs, most of which were going into workstations. Then, graphics chips generated the most activity, and later router chips. With the Darwinian nature and rapid pace of the industry, many of those products have become resume entries and patent portfolio items, rather than something you can buy at Fry’s Electronics. Nevertheless, the industry continues to grow, and intermittently, to prosper.

The articles

This year, we asked eight presenters to prepare articles for this *IEEE Micro* special issue on Hot Chips. Five of these articles appear in this issue, and the remainder will appear in future issues. (Only space limitations have kept us from presenting even more articles based on Hot Chips presentations.)

Ambitious and interesting new chips are not limited to large systems or the most powerful workstations and PCs. We present two articles
describing the architectures and chips that are the basis of the PlayStation 3 and the Xbox 360.


Power efficiency is an important aspect of most new architectures and implementations. It is implicit in the multiple processing designs of the CELL and Xbox 360. A number of presentations at Hot Chips 17 concentrate on power issues and explore new areas to improve efficiency. “Digitally Assisted Analog Circuits,” by Boris Murmann, describes how low-complexity analog building blocks can be enhanced with digital circuits to create high-performance, high-precision analog capabilities such as A/D conversion with substantial power savings. The article “Low-Power, Networked MIMD Processor for Particle Physics,” by Volker Lindenstruth, describes a large, mixed analog and digital system with 283,392 processors on 70,848 chips where power efficiency is an essential design aspect.

New and speculative technologies are always a part of Hot Chips. “CMOS Photonics for High Speed Interconnects,” by Cary Gunn, describes optical transceivers fabricated monolithically with SOI CMOS circuitry on the same die. They are used to implement optical communications capability for high bandwidth LAN, SAN, and chip-to-chip communications.

Field programmable and reconfigurable processing is a special focus of Hot Chips 17. Two articles that cover this area will appear in future issues. “A Software Configurable Processor Architecture,” by Ricardo Gonzalez, describes the Stretch architecture. “A High-End Reconfigurable Computing System and Design Environment,” by Chen Chang et al., describes the Berkeley Emulation Engine 2 (BEE2) and its application to problems in radio astronomy. “CELL Broadband Engine Interconnect and Memory Interface,” by Scott Clark et al., will also appear in a future issue.

Overall, we think that the products, analyses, research, and thoughts presented at Hot Chips each year represent some of the most exciting work occurring anywhere in the world. This work drives our standard of living and prosperity; without technology, we’d be communicating with smoke signals and using water buffalo instead of tractors and combines. We’re privileged to present this special issue of Hot Chips, and we hope that you’ll enjoy this material as much as we have.

John Sell is an architect and silicon lead for Xbox at Microsoft. He has a background in processors and graphics as a senior fellow at Advanced Micro Devices, CTO of The 3DO Company, and a distinguished engineer and chief architect of the initial PowerPC architecture and chips for Apple in partnership with IBM and Motorola. Sell has an MS in electrical engineering and computer science from the University of California, Berkeley. He is a member of the ACM and Siggraph. Sell was program committee cochair for Hot Chips 17 and is the conference vice chair for Hot Chips 18.

Alan Jay Smith is a professor in the Computer Science Division of the Department of Electrical Engineering and Computer Sciences at University of California, Berkeley. His research interests include analyzing and modeling computer systems and devices, computer architecture, and operating systems. Smith has a PhD degree in computer science from Stanford University. He is a fellow of the IEEE, the ACM, and the American Association for the Advancement of Science. Smith received the 2006 Harry Goode award of the IEEE Computer Society and the 2003 A. A. Michelson Award of the Computer Measurement Group (CMG). He was program committee cochair for Hot Chips 17 and is currently chair of the conference’s steering committee.

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