



High performance at affordable power

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.....The fact that energy efficiency is a key design constraint in the late CMOS era is now very well known. Indeed, it is such a critical aspect of chip and system design that the editorial board and I have devoted at least one *IEEE Micro* issue each year to this general topic. There are, of course, at least two ways of looking at energy-efficient design: meeting a power consumption target at acceptable performance, or meeting a performance target at an acceptable power level. Depending on whether the recurrent energy cost (manifested as electricity bills or battery life) or the dissipation (cooling) cost (manifested as the price of the chip package or the overall server system installation) is the dominant consideration, you might view things a bit differently. And, related to this is also the issue of *average* power versus *maximum* power. Nonetheless, at the end of the day, regardless of what chip a team is designing, energy efficiency is probably one of the most important crite-

ria; and, to a lesser or greater extent, both of the viewpoints mentioned are probably present in the designer's field of vision. So, without getting hung up on what the correct perspective ought to be, it is probably fair to say that each designer is interested in understanding and practicing energy-efficient design principles.

Achieving high performance at affordable power (and therefore, cost) is the overall system goal across a whole range of products that serve the home, entertainment, scientific, and commercial-enterprise segments of the information technology industry. And, actually that has always been the goal! The only problem is that growth in the performance-cost ratio (at historical rates) is no longer economically sustainable without major innovations and design paradigm shifts. The trend toward multicore chip designs is an example of a major shift. Pervasive clock gating, and its integration into the basic design methodology and toolset, is an example

of innovative engineering that has now come of age even in high-end systems. Many more new innovations are now beginning to transition from research to real designs, as we enter an era of design where *efficient* use of on-chip and system resources is a concept that will be pursued with an intensity of focus that has never been as strong in the history of CMOS-based design.

I hope the selection of articles in this issue of *IEEE Micro* will bring some of the latest innovations and ideas in energy efficiency to our readers' attention, and thereby foster further thinking and research to improve upon current design practices.

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Editor-in-Chief

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