



Adapting old paradigms to meet new challenges

PRADIP BOSE

pbose@us.ibm.com

..... A familiar problem faced by an architect or designer is how to adapt an older solution or paradigm to fit the constraints imposed by the emerging new challenges in the underlying technology. As such, it is useful to first understand what these challenges are, and how imminent is their impact on reshaping existing architectural paradigms. By the same token, it is also productive to stand back and look at some old design paradigms to see if they would still stand the test of time in future processor development, in light of the upcoming technological barriers. In this issue, we have a blend of articles: some that look ahead to future problems and some that reexamine the past to investigate the future use of known solution approaches.

Some of the most pressing future challenges in microelectronics center around maintaining circuit reliability in the face of shrinking transistor size. In "Trends and Challenges in VLSI Circuit Reliability," Cristian Constantinescu of Intel surveys the effect of deep-submicron technologies on three classes of faults: permanent, intermittent, and transient. In one example, he shows how manufacturing residuals can induce intermittent faults. A second example shows how timing violations can cause subtle computational errors. He presents some data from a case study that detected the presence of this *silent data corruption* and suggests techniques for improving circuit reliability.

"Microcode Processing: Positioning and Directions," Stamatis Vassiliadis, Stephan Wong, and Sorin Cotofana (Delft

University of Technology, Delft, The Netherlands) examine the past use of microcode. Calling microcode "one of the most important innovations" in computer engineering, these authors summarize four principles for the design of microcoded machines. Although they identify advances in technology that bring microcode's place into question, these authors still see its continued usefulness in the area of custom computing machines. They present some results showing that processors augmented with microcoded FPGAs can achieve improved performance on certain media benchmarks.

A growing problem is inherent in today's communication systems: constantly changing protocols. Helping systems adapt to them will be an important task, and the article "A Programmable State Machine Architecture for Packet Processing," addresses this problem. The authors—Wangyang Lai (Agere Systems) and Chin-Tau Lea (Hong Kong University of Science and Technology)—argue that programmable state machines can provide the flexibility necessary to deal with these changing protocols. This article explains their PSM architecture, which includes a simple instruction set.

The issue of the widening gap between memory and CPU performance is a familiar and old one to all computer architects. In "A Case for Studying DRAM Issues at the System Level," Bruce Jacob (University of Maryland, College Park) observes that the DRAM design community has not employed several performance-improving techniques long used by microprocessor

designers. He sees the use of architecture- and system-level techniques on DRAMs as necessary to closing the gap.

"Strategies for Mapping Algorithms to Mediaprocessors for High Performance" presents data on mapping algorithms for two common image-computing functions to a target mediaprocessor, in this case, one from the TMS320C64x series. Based on these results, author Kerem Karadayi (University of Washington, Seattle) and his colleagues from the University of Washington, Texas Instruments, and MicroTechnology claim that mediaprocessors such as the C64x can achieve performance comparable to that of ASICs while remaining programmable and multifunctional.

IEEE Micro is also pleased to present a special panel from the 30th International Symposium on Computer Architecture. In "The Use and Abuse of SPEC: An ISCA Panel," moderator John Hennessy and panelists Daniel Citron, David Patterson, and Guri Sohi discuss the "crime" of subsetting the SPEC benchmark suite. Citron points out that many researchers use only a subset of SPEC; he and the others consider what reasons people might have for doing so. The topic made for a lively and entertaining discussion.

Looking ahead, the next issue of *Micro* deals with two other technological challenges of the future, namely, power consumption and design complexity. The editorial board and I hope you enjoy the blend of issues, challenges, and solution approaches discussed in here, while looking forward to the upcoming theme issue on power- and complexity-aware design.