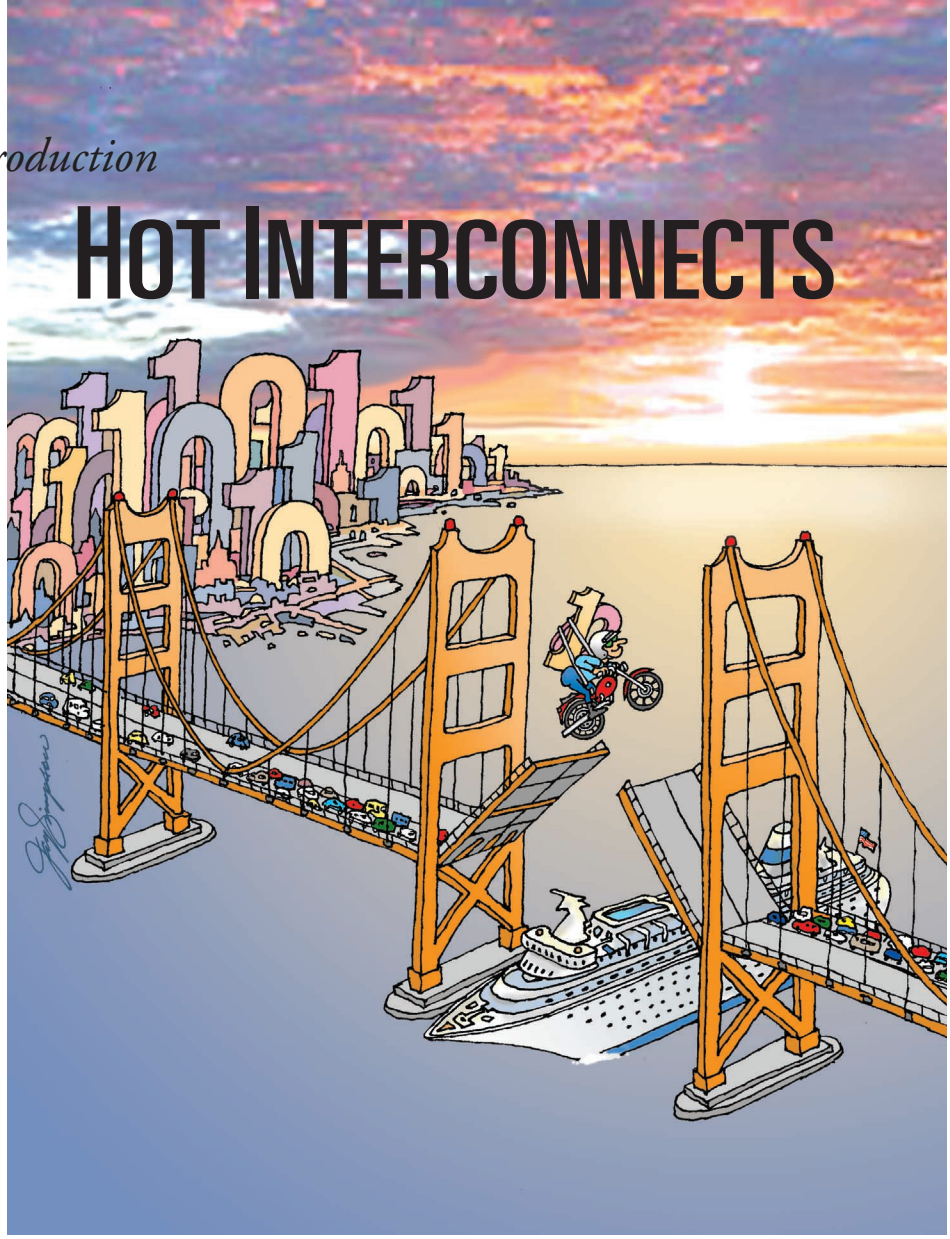
Guest Editors' Introduction

HOT INTERCONNECTS



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The Hot Interconnects conference at Stanford University once again attracted an excellent collection of ideas on high-performance interconnects. This year, the conference received a record number of submissions and provided a full program on current research-related universal services over packet networks. The conference covered many facets of interconnects, including switching systems, multiprocessor interconnects, storage systems, and Internet technology. In this special issue of *Micro*, we present outstanding articles from the 2001 Hot Interconnects 9 conference.

Conference presenters addressed several advances in switching. The use of the input-queued architecture has made single-chip switching elements a practical alternative for interconnecting high-performance systems. A challenge remains in optimally scheduling packet transmissions on these devices. Although finding a maximum-weight match between input ports and output ports achieves optimal transmission assignments, the process requires a great deal of chip area and processing time. In "Efficient Randomized Algorithms for Input-Queued Switch Scheduling," Shah et al. present new, efficient randomized algorithms that show how an approximate matching can run in linear time in proportion to switch size. In "An Implementable Parallel Scheduler for Input-Queued Switches," Giaccone et al. demonstrate another technique by which a parallel scheduler can find near-optimal matching within a single packet transmission cycle.

As multiprocessor systems become commonplace, the interconnects between processors become critical to achieving high performance. Mukherjee et al. present the "The Alpha 21364 Network Architecture," which

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demonstrates how the scalable interconnect can maintain coherent, directory-based cache coherence for up to 128 processors. Next, in "The Sun Fireplane Interconnect," Charlesworth shows how this interconnect uses multiple snoopy buses to preserve low-latency access to shared memory. Petrini et al. present "The Quadrics Network: High-Performance Clustering Technology," which lets clusters of workstations maintain a global virtual-address space and fault tolerant communication.

As the Internet grows, it needs new technology to route, process, manage, and transport the increasing volume and variety of data. One approach to scaling the route lookup process is to algorithmically reduce the size of the tables used to hold the routes. In "Routing Table Compaction in Ternary CAM," Liu presents a technique to implement reduction with commonly used ternary content-addressable memory. For a router to fully process an Internet datagram, it must examine multiple protocol layers within the packet header. "Protocol Wrappers for Layered Network Packet Processing in Reconfigurable Hardware," by Braun et al. presents a library of synthesizable protocol wrappers that efficiently implements packet header processing in hardware. To monitor network traffic, a router must maintain detailed statistics about events that occur while processing data. Typically, on-chip counters or off-chip memory is used to track events as they occur in the switching elements and packet processors within the router. As the number of statistics and the rate at which the events occur exponentially increase, traditional techniques of tracking statistics become infeasible. "Maintaining Statistics Counters in Router Line Cards," by Shah et al., presents a technique that implements all of these counters using only one external memory and a small cache of on-chip memory.

The last article in this special issue considers how new optical technology can aid Internet switching. Although circuit switches lend themselves well to optical implementations, packet switches generally do not. In "TCP Switching: Exposing Circuits to IP," Molinero-Fernández and McKeown present a method in which TCP/IP flows trigger the creation of optical circuits in the underlying network. The technique provides an evolutionary path that migrates Internet services to optical networks.

Several individuals helped make the 2001 Hot Interconnects conference a success. Fred Bauer served as the general chair and provided outstanding leadership in the conference's organization. Ibrahim Matta organized the tutorials and panels. We thank Bruce Davie for moderating the Multiprotocol Label Switching (MPLS) panel and Bob Hinden for leading the IPv6 panel. We also appreciate the efforts of Zhi-Li Zhang, Melanie Swan, Bob Wedig, Liz Rogers, and Eric Cheng for their help on the executive committee.

We look forward to another great conference in 2002. Hot Interconnects 10 will be held again at Stanford University. The program committee looks forward to submissions on research topics that advance the architecture and implementation of interconnect technologies. More information about the Hot Interconnects conference is available at http://www.hoti.org.

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