Interconnecting communicating entities is one of the fundamental problems in computer science and engineering. Interconnection problems occur at various levels—between gates in a chip, between chips on a module or board, between boards across a backplane, and among autonomous computer systems that may span large geographical areas. The complexity of interconnections often has a profound influence on the cost, performance, and reliability of the resulting system.

This special issue of IEEE Micro features six articles on the topic of interconnection and networking, drawn from the papers presented at the Seventh IEEE Hot Interconnects Symposium held at Stanford University in August 1999. The annual Hot Interconnects is held as a companion to the IEEE Hot Chips Symposium. Hot Interconnects covers a large spectrum of interconnect topics, from circuit-level technology to network architectures and protocols. The organizers particularly direct the sessions at new, exciting product and technology innovations in these areas. This year’s symposium featured presentations on network switching and routing, optical interconnects and networking, network-attached storage systems, system-level I/O interconnect tech-
The six articles included here represent a cross section of the 22 papers presented at the symposium. The articles address interconnection and networking problems at various levels and in different contexts. The first article, “Architectural Considerations for CPU and Network Interface Integration,” discusses the design of efficient network interfaces. This problem is becoming increasingly important because of the range of devices that are being connected to the Internet. Achieving the desired performance at a low cost requires the integration of processing and interface functions on the same chip. The authors propose an architecture that integrates network interface functions with a processor and evaluates its performance in two example applications.

A critical function that needs to be performed within every packet switch or router is address lookup. This function is responsible for determining the outgoing link to forward an incoming packet, based on address information contained within the packet. When forwarding occurs at the IP (Internet Protocol) layer, the operation is more complex than a flat lookup of an address to yield the forwarding information. The routing table in an IP router or switch is usually organized as a set of address prefixes, and the function of the lookup algorithm is to determine the longest prefix in the table that matches the destination address of the incoming packet. The recent literature has proposed many algorithms for the efficient determination of such longest prefix matches. The “Cache Memory Design for Internet Processors” article proposes the caching of address ranges in the lookup table as a solution to the problem and evaluates the trade-offs involved.

Packet classification is another important problem in the design of routers and switches, where one or more header fields of an incoming packet are matched against a set of rules to determine its class. Packet classification may be necessary for several reasons (service differentiation, service guarantee provisions, policy enforcement, congestion control, and load balancing). This function is becoming increasingly important because of the need for supporting multiple types of traffic in packet networks. Because of the need to classify packets along multiple dimensions, the problem is computationally demanding. However, the recent literature has proposed a number of algorithms to provide this function in switches and routers. These algorithms make trade-offs among the classification time, size of the data structure maintained by the algorithm, and time needed for preprocessing the rule database into the internal data structures.

In “Classifying Packets with Hierarchical Intelligent Cuttings,” the authors observe that deterministic algorithms to solve the general packet classification problem can be too expensive for large rule bases and propose heuristic algorithms as an attractive alternative. Their approach is to divide the space in each dimension recursively into intervals and organize the rules that fall into each interval as the nodes in a tree. The partitioning is done such that the number of rules represented by each node in the tree is within a set limit. This can result in an efficient search tree for a given set of rules, making the classification fast. However, the drawback is the long preprocessing time to generate the data structure. The approach is attractive when the rules do not change frequently, so that the data structure will not need to be updated often.

Traffic scheduling is yet another function supported by current-generation switches and routers. The function of a traffic-scheduling algorithm is to determine the relative priorities among the packets that are competing for transmission on an outgoing link. These algorithms are necessary for providing bandwidth and delay guarantees to packet streams, and for the fair distribution of resources in the network. The authors of “A Scheduler ASIC for a Programmable Packet Switch” describe the implementation of a scheduling algorithm in a chip designed at the University of Toronto.

The last two articles deal with I/O interconnection. The first, “Authenticating Network-Attached Storage,” concerns the attachment of a storage device directly to a computer network such as a LAN (local-area network). This eliminates the need for specialized standards and protocols for I/O interconnection. However, computer networks are much more accessible and much less secure than I/O networks, and require authentication mechanisms to maintain the integrity of the I/O system in an open network environment. The authors propose solutions to this problem.
The final article evaluates the IEEE-1394 serial bus, which is widely used for the interconnection of consumer electronics equipment such as camcorders to personal computers. In "An Empirical Analysis of the IEEE-1394 Serial Bus Protocol," the authors provide insights into the operation of the IEEE-1394 bus protocols from measurements performed on several system configurations, using an analyzer they designed.

Hot Interconnects 8 will meet once again at Stanford University in 2000. For information, visit the symposium Web site at www.hoti.org.

Acknowledgments
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Call for Contributions
Hot Interconnects 8
August 16-18, 2000 Stanford University
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Hot Interconnects is an international symposium focusing on the hardware and software architecture and implementation of high-performance interconnects of all scales. The theme of the year 2000 meeting addresses the cross-cutting issues spanning computer systems and networking technologies for providing universal services over packet networks.

Example topics include optical networking, network-attached storage, transport of emerging services over packet networks, high-performance network interfaces, wireless interconnects, novel switching and routing technologies capable of providing differentiated services, plug-and-play network interfaces, and active network architectures. The conference is directed particularly at new and exciting product and technology innovations in these areas. Contributions should focus on real products, prototypes, or experimental systems and their performance evaluation.

Access the complete Call for Contributions and more information on the symposium at www.hoti.org.