

THE INCREASINGLY IMPORTANT INTERCONNECT

..... This special issue of *IEEE Micro* features five articles drawn from presentations at the sixth annual Hot Interconnects Symposium held at Stanford University in August 1998. The symposium accepts both presentations and full papers, and attracts significant involvement from both industry and academia.

Originally organized as a companion to the popular Hot Chips Symposium also held at Stanford, Hot Interconnects' primary goal is to present innovative new technologies, be they intrachip, between chips, between boards, between systems, or between countries. The symposium covers electrical and optical interconnects, network interconnects, switches and routers, networked file systems, and the Internet itself.

Interconnects are becoming increasingly important: many highly complex chips today are limited in area, power, and delay by the available interconnect technology. The size and power of computer and network systems are often limited by the speed and power of interconnects between board, subsystems, and equipment shelves. In addition, the Internet is built around interconnects between enterprises, data exchanges, and carriers. As interconnects have grown to great significance in chip, boards, system, and network design, so has the Hot Interconnects Symposium grown to include members of the semiconductor, computer, networking, and research communities.

In this issue we feature articles that represent the diverse nature of this field. We begin with three articles about fast switching. The first describes a 26.8-Gbyte/s crossbar switch developed by Hitachi. Note that the bidirectional transceiver design permits simultaneous transfer of data in both directions of a

single link. This technology is of particular interest in systems with dense interconnects and a short supply of packaging and connector pin counts.

Next is an implementation of a crossbar scheduling algorithm for the Tiny Tera switch at Stanford. The initial system architecture was first described at Hot Interconnects in 1996 and appeared in *IEEE Micro* in January 1997. Our current article considers how to implement a fast, fair, and efficient arbitration algorithm for a single-stage 320-Gbps crossbar switch.

The third article also completes work introduced earlier at Hot Interconnects. Atlas I is a single-chip ATM switch developed by university researchers in Greece. Earlier descriptions presented the original architecture through the implementation process, and now we see the results of this work. In the competitive field of networking, detailed and rigorous evaluations of the engineering trade-offs required to build real network switches are rare. The authors provide a unique glimpse into the process; it is a must read for anyone contemplating building a network switch or router, or a multiprocessor interconnect.

Then, we move to articles on system-level interconnects, starting with the implementation of highly available file server appliances. By examining a technology approach to minimize disruption of service due to hardware faults, the authors address reliability, availability, and serviceability (RAS) in a server-based network. The architecture and technology use a clustered failover approach to the design of the network.

Finally, we look at a much larger problem by addressing some of the issues of perfor-

Nick McKeown
Stanford University

Chase Bailey
Cisco Systems

mance in the Internet. An ongoing research program at the University of Washington examined the networks' ability to exploit computational resources in the network to reduce congestion and latency, and improve routing. This article is a very good representation of the symposium's approach to promoting new and very interesting ways to introduce leading-edge research on algorithms for interconnects at the very highest scale.

We hope that you find these articles as exciting as we have; they represent the state of the art as well as a cross-section of this growing field.

Hot Interconnects will be held once again at Stanford in 1999, and we encourage you to participate. For more details, visit <http://www.hoti.org>.

MICRO

Nick McKeown is a professor of electrical engineering and computer science at Stanford University. He works on the theory, design, and implementation of high-speed Internet routers and switches. He has worked for Hewlett-Packard Labs and Cisco Systems, and currently is on leave at Abrizio Inc. McKeown

completed his PhD at the University of California, Berkeley. He is an editor of the *IEEE Transactions on Communications*, the Robert Noyce Faculty Fellow at Stanford, and a research fellow of the Alfred P. Sloan Foundation.

Chase Bailey is the principal technologist at Cisco Systems in San Jose. His responsibilities include the assessment and analysis of emerging technologies, and how they relate and can be incorporated into the company's current long-term strategies. He is an adjunct professor at Santa Clara University in the graduate program, School of Computer Engineering. He also leads the University Research Program and Research Review Board, where his major focus is the funding of research projects with leading universities. Previously, he was founder, chairman of the board, and chief technical officer of Efficient Networks. Bailey holds a BS from Albany State College and is a member of the IEEE, IETE, and ACM.

Direct comments about this special issue to Nick McKeown, Computer Systems Lab, Gates Building 3A, Room 351, Stanford University, Stanford, CA 94305-9030; nickm@stanford.edu.

COMING IN THE MARCH-APRIL 1999 *IEEE MICRO*

Special Issue on the 1998 Hot Chips Symposium

The next issue of *IEEE Micro* features selected articles drawn from presentations at the 1998 Hot Chips Symposium. Guest Editors Norm Jouppi (DEC) and John Wawrzynek (Univ. of California, Berkeley) are preparing a Hot Chips feast for you. You will find fact-laden articles discussing

- ✓ Deep Blue's chess grandmaster chips
- ✓ Ultra Sparc III
- ✓ Neon: A 256-bit graphics accelerator
- ✓ Alpha 21264 microprocessor
- ✓ AMD 3DNOW!
- ✓ IBM S/390 G5 microprocessor
- ...and even more!

Be sure to read the March-April 1999 issue of

IEEE
MICRO
Chips, Systems, Software, and Applications